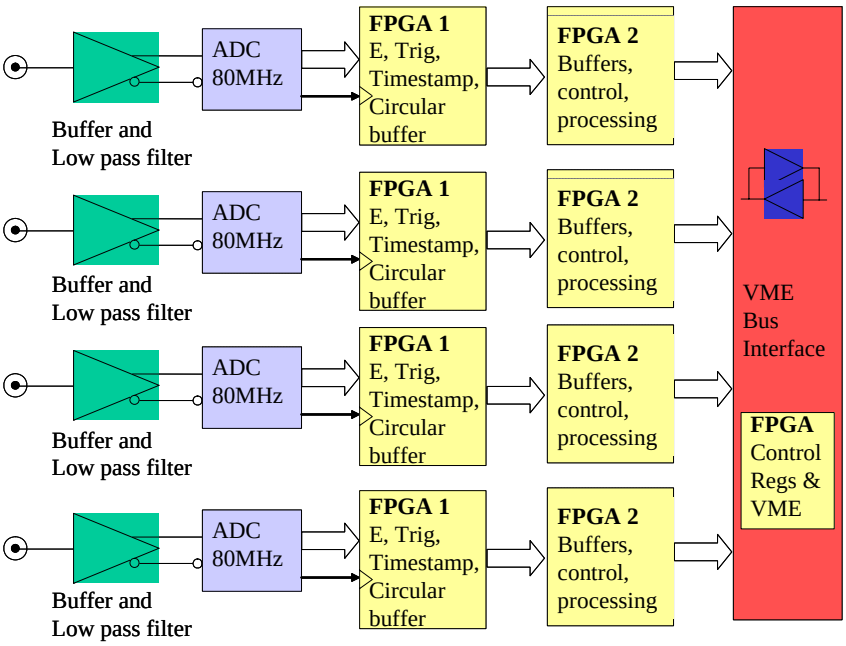
GRT Card. Manual (version 3 revised Aug 2006)

Block Diagram:



1 Input sensitivity and architecture:

1.1 Channels in non-differentiated (switch closed):

Gain is x2; ADC maximum range is 1.1Vpk-pk on each side of the differential pair, i.e. 2.2vpk-pk, so the input limit is 550mV terminated, 1100mV unterminated, equivalent to 5.5MeV for 200mV/MeV preamplifier sensitivity.

1.2 Channels in differentiated (switch open):

Full scale (±550mV into ADC) equates to 15mV/ns input change, equivalent to 750mV terminated, 1.5V unterminated input voltage change in 50ns (equivalent to 7.5MeV for 200mV/MeV sensitivity)

1.3 Channel Architecture

- Between input and ADC are a 40MHz bandwidth low pass filter and optional differentiator
- Inputs are terminated in 50ohms internally.

1.4 ADCs

The ADCs are 14 bits, 80 MHz accepting bipolar inputs and producing 2's complement data.

1.5 Timestamps

The timestamps are driven from the VME Sysclk - i.e. clocked at 16MHz (62.5ns) from a common clock to all cards within a single VME crate.

1.6 Trigger Inputs/Outputs: 3 SMA Connectors

- Trigger In (Fast NIM)
- Trigger Out (can be changed under s/w control to be used as “busy/buffers full” output (Fast NIM))
- Gate In (can be used either as trigger gate or else to synchronise timestamps) (Fast NIM)

2 VME Interface

Warning: *The GRT4 cards have an unusually large number of decoupling capacitors which affect what happens when power cycling the VME crate. Leave the crate turned off for about 1 minute to be sure that the capacitors are fully discharged before turning it on again. Failure to wait long enough will result in one or more FPGA failing to load, The FPGAs contain the VME interface and the registers described below, so if they are not programmed then the registers will not exist! Each FPGA will light one of the 9 LEDs at the front of the card when it has successfully programmed.*

2.1 Data Bus

The module uses the bottom 16 data bits, so word access is preferred.
Longword access is allowed, but only the bottom 16 data bits, D15-D0, are read or written.

2.2 Address Modifiers

Module uses AM9 or 13 for single cycle, AM11 or 15 for block transfer (User and supervisor, extended address)

2.3 Bus Error:

Reading or writing using longword access with A1 set (odd word boundary) generates a bus error.
Block transfer write cycles generate bus errors: block transfer mode is read only.

2.4 Register Access inside the GRT4

The GRT4 uses one common data bus internally to access registers and also to transfer data between the 2 FPGAs. There is bus contention logic inside the GRT4 which gives priority to data access. In this case a VME write is ignored (although DTACK is returned as normal) and a VME read will return 0xFFFF. Therefore the GRT4 registers and parameters cannot be reliably adjusted while the card is collecting data. The potential for problems is proportional to the count rate.

In order to adjust parameters safely, the front panel gate should be used to control triggering (see section 4). Alternatively, in the case of external triggers, the trigger input can be switched off by a relay or by disconnection. The GRT version of MIDAS controls VME relay cards type XVME260.

2.5 Addressing:
Base address is set by switches (16) on address lines A31-A16. A15-A1 are decoded according to the following table:
A15, A14 decode to select channel. A13 selects registers (0) or FIFO (1). A12 selects DPP LCA (0) or ADC LCA (1)

Function	**Channel A**	**Channel B**	**Channel C**	**Channel D**
Rd/Wr DPP CSR Reg	Base+0x0000	Base+0x4000	Base+0x8000	Base+0xC000
Rd only DPP write ptr	Base+0x0002	Base+0x4002	Base+0x8002	Base+0xC002
Rd only DPP read ptr	Base+0x0004	Base+0x4004	Base+0x8004	Base+0xC004
Rd only DPP Version	Base+0x0006	Base+0x4006	Base+0x8006	Base+0xC006
Rd/Wr DPP Reg 5	Base+0x0008	Base+0x4008	Base+0x8008	Base+0xC008
Rd/Wr DPP Reg 6	Base+0x000A	Base+0x400A	Base+0x800A	Base+0xC00A
Extended DPP address	Base+0x08XX	Base+0x48XX	Base+0x88XX	Base+0xC8XX
Rd/Wr ADC CTRL	Base+0x1000	Base+0x5000	Base+0x9000	Base+0xD000
Rd/Wr ADC Pretrig	Base+0x1002	Base+0x5002	Base+0x9002	Base+0xD002
Rd/Wr ADC Header	Base+0x1004	Base+0x5004	Base+0x9004	Base+0xD004
Rd/Wr ADC Trigger	Base+0x1006	Base+0x5006	Base+0x9006	Base+0xD006
Rd only ADC Version	Base+0x1008	Base+0x5008	Base+0x9008	Base+0xD008
Rd/Wr ADC Spare 4	Base+0x100A	Base+0x500A	Base+0x900A	Base+0xD00A
Extended (MWD) address	Base+0x18XX	Base+0x58XX	Base+0x98XX	Base+0xD8XX
Data FIFO Read only	Base+0x2000	Base+0x6000	Base+0xA000	Base+0xE000

For addresses with A11 set, address lines A1-A8 are passed to the ADC (MWD) and DPP LCA and used to decode extra addresses under control of bits A14,A15 to choose channel and A12 to select between ADC/DPP LCA. A1-A8 are carried on common_sp11-18 respectively. Common_sp10 is set to 1 to enable this extended addressing mode when A11 is 1 and when not reading the FIFO (A13=0). (Only true from v5a of VME interface LCA onwards.)

Data FIFO: read returns 16 bits of output data in D0-D15 at any of the 4k words (0x2000-0x3FFF in Ch A etc.)

Data format:

D15(msb) D0(lsb)
Header+Counter
Timestamp High
Timestamp Mid
Timestamp Low
ADC Sample 1
…
ADC Sample 250
*Energy Word **
*Baseline Word **

* order of energy and baseline words depends on DPP reg 5 setting. Also the msb may be replaced by the pileup bit under the control of ADC Trigger register bit 2.

2.6 Registers:

DPP CSR reg

bit 0 puts the ADC header word into the output buffer for each trace if set to 1 (= 0xffff if 0)
bit 1 puts timestamp d47-32 into the output buffer for each trace if set to 1 (= 0xffff if 0)
bit 2 puts timestamp d31-16 into the output buffer for each trace if set to 1 (= 0xffff if 0)
bit 3 puts timestamp d15-0 into the output buffer for each trace if set to 1 (= 0xffff if 0)
In normal operation bits 0,1,2,3 will be set to 1.

bits 4-6 not yet defined. Can be read and written.

Bit 7 indicates that the channel is not in use (so readout should skip it) 1= not in use, 0=normal

Top 8 bits are status so writes on d8-d15 are ignored.
Bit 8 (read only) Buffer Empty when read as 1
Bit 9 (read only) Input paused because buffer is full *(doesn't restart until the buffer is empty)*
Bit 10 (read only) Reading last word from buffer.
Bits 11-15 not yet defined: always read 0.

DPP Write ptr

The write pointer for the data buffer. *(Read only)* (Value is latched at start of Data Strobe)
Note that the top 5 bits are not used for addressing because the output buffer is only 2k x 16.

DPP Read ptr

The read pointer for the data buffer. *(Read only)* (Value is latched at start of Data Strobe)
Note that the top 5 bits are not used for addressing because the output buffer is only 2k x 16.

DPP Version

16 bit version number (upper byte = major release, lower byte = revision)

DPP reg 5

D0-D7 used for selecting MWD data order (set 4 bits address for accessing MWD local regs)
0x00ef puts energy in EOH and baseline in EOL spectrum. 0x00fe puts energy in EOL, baseline in EOH. Other values are all invalid.

DPP Reg 6

trace length in 16 bit words (including header and MWD).
(0 is interpreted as 512 for backwards compatibility.
Normally traces are 256 long, so register =0x0100)

NB length of traces written to the output buffer is not affected by turning on/off the 6 header words in DPP CSR register. So number of data samples= (tracelength-6) words.

ADC CTRL Register

bit 0 Soft Reset (level sensitive- resets as long as it is set to 1 and released when set to 0).
Soft Reset sets all FIFOs, buffers, counters, pointers to zero, clears the timestamp and trigger counter to 0 and resets all readout logic. It doesn't affect the registers defined here except where the resets change what is reported in the status about buffer full/empty status. Soft Reset also resets all LCA clocks, forcing them to resynchronise. Hard reset is derived from VME sys reset or the hardware reset switch. This has the same effect as soft reset, but in addition it clears all the GRT registers described in this section to 0.

Bit 1 is the "Go" bit which gates the triggers. If Go is 0 then triggers are disabled and no data are collected. Normally Go is set to 1 (i.e. active)

Bit 2 controls whether timestamp counters are reset by the gate input (1= reset by gate, 0 = ignore gate) *If bit 2 = 1 then bit 3 becomes significant and must be programmed.*
Bit 3 controls which polarity of gate resets timestamp (only used if bit 2=1). 1= reset when gate input is active (-4mA, Fast NIM 1); 0 = reset when gate input is inactive (0v Fast NIM 0)).

Bit 4 controls whether the counter in the header word increments for all triggers (0) or only accepted triggers (1) *(Triggers are not accepted during Inhibit/busy).*

Bit 5 controls whether Trigger Out on the front panel is Trigger Out (0) or Busy/Inhibit (1).
If its Trigger then trigger register bit 10 is used to define what is OR'ed into the trigger out.
If its Busy/Inhibit then its driven by the OR of all the channels' Inhibited (busy) logic.
NB bit 5 must be set to the same state in all channels- failure to do this will make the Trigger Out meaningless.
Bit 6 controls polarity of Inhibit/busy output. 1 inverts it; 0 doesn't invert **(Exists only in ch D)**

Bit 7 controls which polarity of gate is used when gating triggers. 1= allow triggers when gate input is active (-4mA); 0 = allow triggers when gate input is inactive (0v).
(Gating triggers is enabled and disabled by trigger register, bit 8)

Bit 8 controls whether trapezoid energy is read with (0) or without (1) baseline subtracted.
Normally set to 0 but sometimes useful not to subtract baseline for diagnostics

Bits 9-10 Digital gain control (x1 to x8).
Selects D31:D16, D30:D15, D29:D14 or D28:D13 from D31:D0 energy and baseline values

Gain	Bit 10	Bit 9
x1	0	0
x2	0	1
x4	1	0
x8	1	1

Bits 11-15 are not yet defined but can r/w them (D11-D15)

ADC Pretrig:

D0-D7 only are used to define pretrigger depth in ADC buffer (256 words deep). R/W access.
D8-15 always read back as 0.

ADC Header:

The header word can be written with every trace (under control of DPP CSR register)
Header bits 0-7 are connected to a counter which increments with every requested trigger or every accepted trigger (controlled by ADC CTRL bit 4).
These bits may be written to preload the counter, but the value read back will depend on whether or not triggers have incremented the counter between the preload and the read.

Header bits 8-15 contain the header byte. This is initially set to 0 and can be read or written.
Note that writes to bits 8-15 will also load the counter with the value in D0-7.
The reverse is true: when loading the counter, the header byte is over-written with the data on D8-D15.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
msb	Trace header byte (read/write)						lsb	msb	Counter (read and preload)						lsb

ADC Trigger

NB- Internal trigger is now a CFD with threshold in another register (ADC Spare 4).
So bits 3 to 7 are no longer needed to define the operation of the old "tendency trigger"

Bit 0 controls whether trigger comes digitally from LCA (1) or front panel trigger input (0)

Bit 1 controls whether internal trigger is looking for a rising edge (1) or a falling edge (0)
(Rising and Falling are defined at the card's input, i.e. for +ve preamp pulses set this bit to 1 and for –ve preamp pulses set it to 0. Traces in GRT4 spectra are inverted with respect to the preamp, so +ve ADC traces should have this bit=0 because the preamp pulse is really -ve.)

Bit 2 controls whether the pileup bit replaces the top bit of energy and baseline (1) or not (0)

Bits 3-7 are no longer used but can still be written and read back.

Bit 8 controls whether the gate input is ignored (0) or required to be active to allow triggers (1)

Bit 9 This bit is only effective when ADC CTRL bit 5 is set to 0. Normally (0) the channel accepts only digital or front panel triggers. This bit allows any other channels on the same card to trigger this channel when set (1) *(bits 12-15 select which channel(s) can trigger this one)*

Bit 10 This bit is only effective when ADC CTRL bit 5 is set to 0. In this case it controls whether front panel "trigger_out" is the same as front panel "trigger_in" (0) or whether any active channels on this card are OR'ed with "trigger_in" to generate "trigger_out" (1).
NB Bit 10 exists but has no meaning in Chan A-C; only channel D drives "trigger_out"

Bit 11 not yet allocated

Bit 12 when set to 1, trigger this channel using chan A "trigger out" signal if bit 9=1.
Bit 13 when set to 1, trigger this channel using chan B "trigger out" signal if bit 9=1.
Bit 14 when set to 1, trigger this channel using chan C "trigger out" signal if bit 9=1.
Bit 15 when set to 1, trigger this channel using chan D "trigger out" signal if bit 9=1.

ADC Version 16 bit version number (upper byte = major release, lower byte = revision

ADC Spare 4 CFD threshold (a good starting point for this is 0x0080)

It is possible to use the front panel "trigger out" to see the CFD's output pulse for setup purposes. For example to see channel A's CFD.

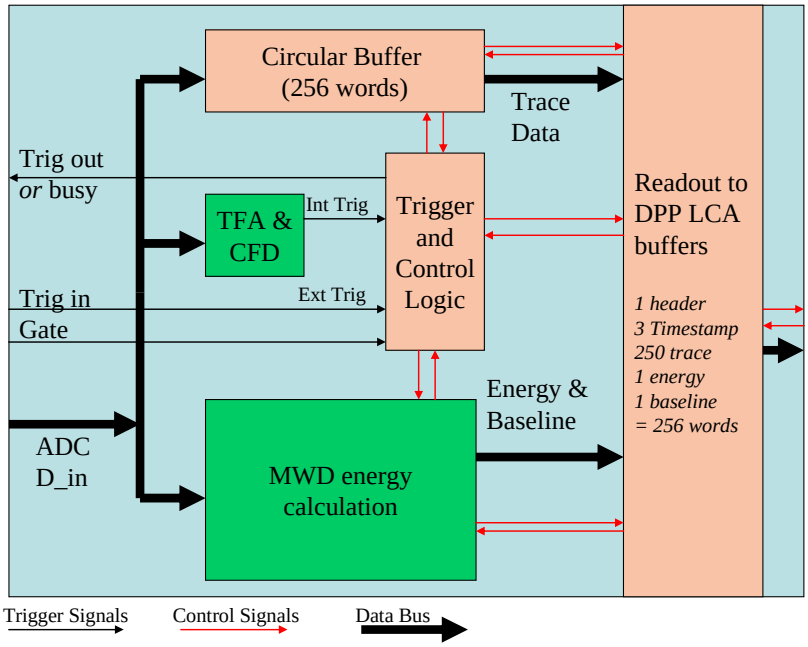
1. *Set internal trigger mode in channel A Trigger register*
2. *(Set d0=1 i.e. set the 0x0001 bit in the trigger register)*
3. *Set all 4 channels to make output trigger, not Busy (set d5=0 i.e. change 0x0020 to 0x0000)*
4. *Set d10=1 in channel D trigger register (NB I do mean D, not A!)*

(set 0x0400 bit). This OR's the internal triggers from A-D with the front panel trigger input to make the trigger out.

Now, disconnect the front panel trigger in, The GRT4 card will only generate trigger out pulses from channel A's CFD which can be used to trigger a 'scope and look at the preamp signal going into the GRT4 (or that signal after a NIM shaper) and then adjust the CFD threshold in the normal way.

3 Algorithm control settings

The diagram below shows the main logic blocks in the ADC (MWD) FPGA and highlights in green the 2 algorithm blocks described in this section.



3.1 Constant Fraction Discriminator (CFD)

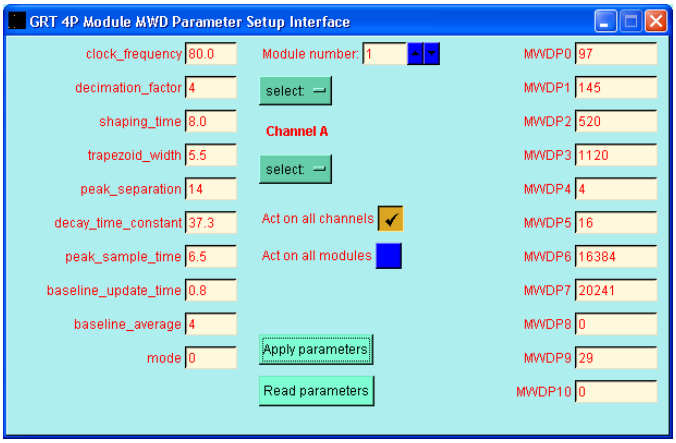
- Delay- fixed (50ns)
- Fraction- fixed (0.5)
- Threshold- programmable ADC Spare 4 register. Typically= 0x0080 = 9mV threshold at input[1]

TFA- not programmable. 250ns rise time, 250ns shaping time (triangular shaping), decimation 2, no BLR and decay time constant fixed at 50us.

[1] This equates to 60keV for 155mV/MeV into 50R (310mV/MeV unterminated). Therefore step size is about 0.5keV.

3.2 Moving Window Deconvolution (MWD)

The MWD code's registers can be accessed by the extended address area (0x18XX etc.) which allows the user to change the shaping time, decay time correction etc. After changing these settings it is necessary to activate and clear the soft reset to force the MWD code to reset and re-read the registers (the MIDAS GUI, see picture below, does this automatically). Some parameters are accessible via registers but actually are fixed by the hardware or the VHDL code- these are marked below as fixed.



Clock frequency- fixed (80MHz)

Decimation factor- fixed (4)

Shaping time- programmable 0 to 12.8us

Peaking time[2]- programmable 0 to 12.8us

Peak separation- programmable 0 to 800us

Decay time constant (PZ)- programmable nominally 50us

Peak sample time- programmable 0-800us

Baseline update time- programmable 0-12.8us

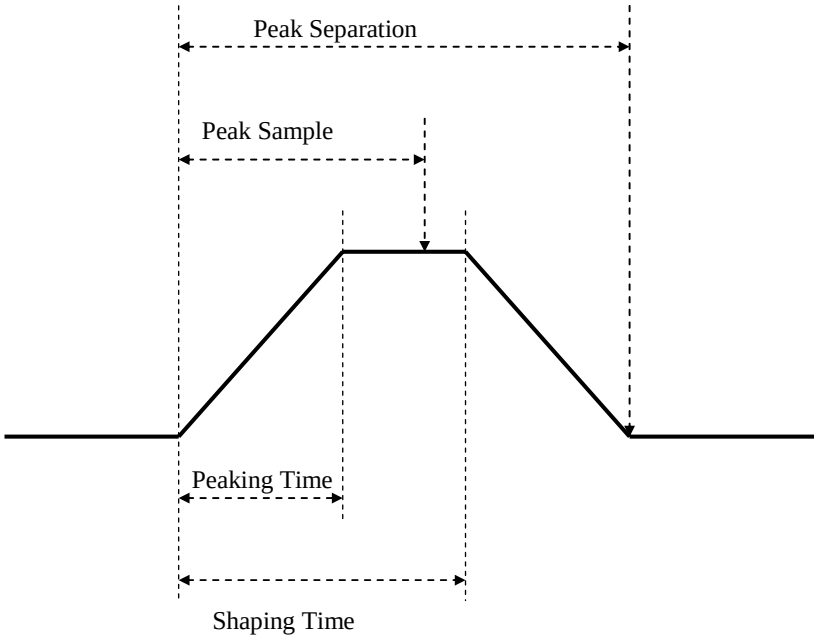
Baseline average- programmable 0-16, (bits 4-7 ignored)

Mode- should normally be 0 (other values are 1,2,3).

The MWD parameters should be programmed as follows:

The 2 fixed values must be programmed to 80MHz clock and decimation of 4. Set mode to 0.

Set the Shaping time, peaking time, peak separation time and peak sample time based on the required filtering. Typical values for the shaping time would be 8us, peaking time 6us, peak separation 14us and peak sample 7.5us. The peak separation should be set to the sum of the shaping + peaking times. The peak sample[3] should be set to a point 75% of the way across the flat top.



[2] MIDAS labels this as "Trapezoid width" for historical reasons. Trapezoid flat top = (Shaping time) - (Peaking time); the trapezoid width (fwhm) is actually the same as the shaping time (shaping time = rise time + flat top).

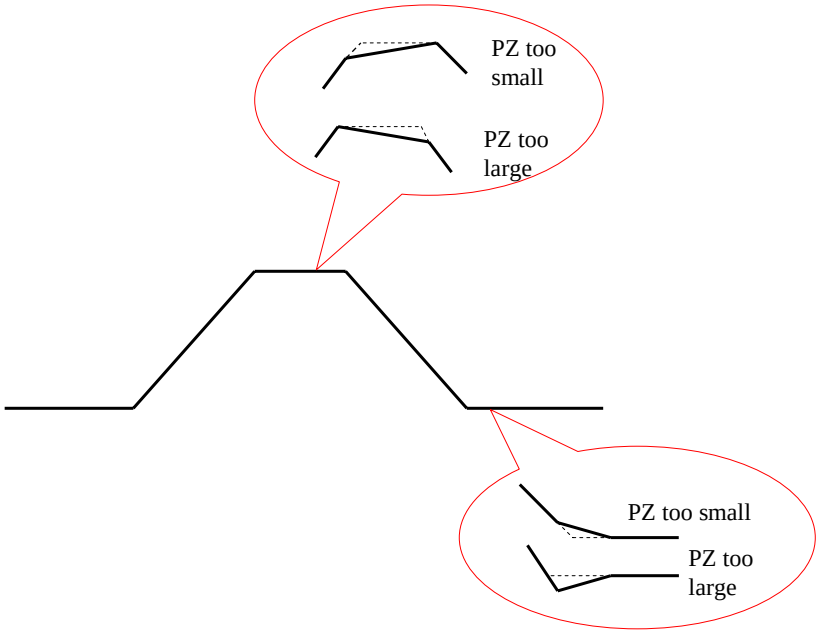
[3] The peak sample time actually starts 500ns after the trigger is detected. This covers the potential problem of the latency in the digital CFD used for pileup detection- 500ns covers the delay between an external analogue CFD causing a trigger and the internal CFD recognising the same trigger after its latency period.

PZ (Decay Time Constant): the MWD algorithm needs to correct for the preamplifier's decay time constant (nominally 50us). If there is only 1 pole then we can make a perfect correction which will result in a totally flat "flat top" to the trapezoid and no over/undershoot at the end of the trapezoid.

In reality most preamps have more than 1 pole and so the PZ adjustment is a compromise.

There are 3 possible ways to adjust the PZ. Normally a combination of 1 as a starting value with 2 to fine tune the value will be sufficient. Method 3 is an alternative (or a check after the first 2).

1. Look at preamp pulses with a 'scope (or using GRT4 traces) and analyse them to calculate the decay time constant. Then program this value into MIDAS software on the MWD parameters window.
2. Run the GRT4 card to collect data and look at the baseline spectrum. Adjust the PZ until the peak in the baseline spectrum is symmetrical.
3. Move the peak sample point from rise time (MIDAS name Trapezoid width) to the shaping time in small steps (0.5us) and measure the peak position of the energy spectrum for each value of the peak sample. The peak position will be constant if the PZ is correctly adjusted and the flat top really is flat. If it is not flat then adjust the PZ (see diagram below) to remove the slope. After doing this, check the undershoot or overshoot at the end of the trapezoid by increasing the peak sample time beyond the shaping time and track the peak position in the energy spectrum as it decreases to the same value as the baseline peak. Plot the energy peak position against peak sample time to look for overshoot and undershoot (see diagram below).



The baseline behaviour is controlled by a combination of the baseline update rate and the baseline averaging. The baseline updating is gated off from the time the CFD detects a pulse for a period of time equal to 2x the peak separation time. After that, if no new trigger is seen, then the result of the trapezoid filter should have returned to the baseline, and values can be used in calculating a baseline average. The update time of the baseline register is typically 1us and the baseline averaging depends on the count rate. At low rates averaging of 4 is possible, but at higher rates an average of 3 is better. The average is applied as a power of 2, so averaging 4 uses 16 samples, averaging 4 uses 8 samples.

Mode controls when energy and baseline values are updated and the normal setting is 0. Other settings are for test and diagnostic use only.

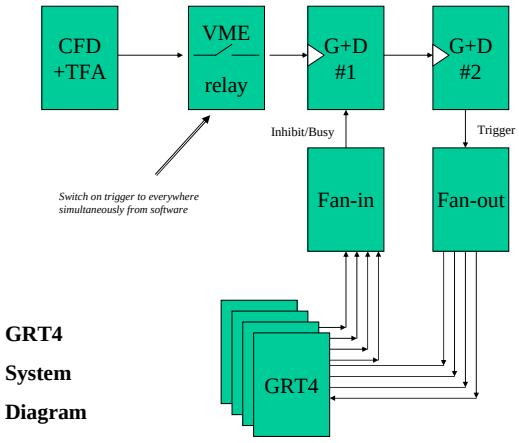
4 Triggering, flow control and starting:

The GRT4 can be triggered externally from a common trigger or internally from the CFD in each channel. This is selected by the ADC Trigger Register. Regardless of the internal/external trigger setting, the MWD's baseline control and pileup detection is always triggered by the CFD, so the CFD must always have a good threshold set.

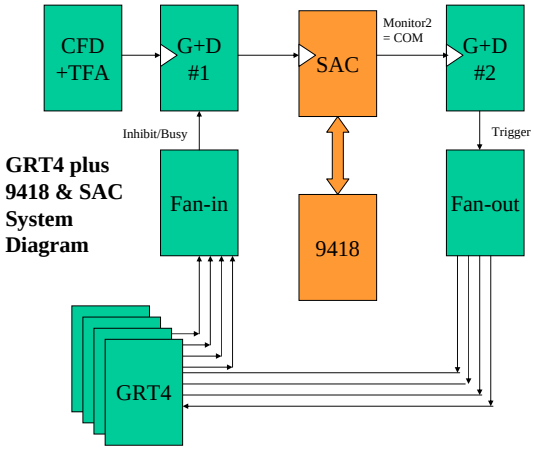
The GRT4 can deal with either positive or negative inputs, however the logic must be programmed to tell it which to expect both for trigger and for MWD energy calculation. The signal polarity is selected in the ADC Trigger Register (the same setting is used for polarity of energy calculations).

Trigger gating. The triggers (internal or external) may optionally be gated by the front panel gate input. Each channel has its own enable/disable bit, but these cannot all be programmed at once, so if the enable/disable bit in the ADC Control registers is used to control acquisition, then there is a delay from the first channel enable to the final channel enabled determined by the VME write times. To overcome this with common external triggers the GRT4 common trigger input may be wired via an XVME260 VME relay card which is only enabled after the last channel enable. If such a relay card is not available then the fast NIM gate signal can be used to ensure that all channels start at the same time (or the trigger can be manually disconnected/reconnected). The gate signal can also be used to reset the timestamp counters simultaneously across all GRT4 cards. With an internal (CFD) trigger the gate is the only way to block or permit triggers and to synchronise the GRT4 cards.

The GRT4 cards have a single fast NIM output which can be programmed to be either Trigger Out or Inhibit/Busy. The Inhibit/Busy signal is used for flow control when a common external trigger is in use. The Inhibit/busy signals are fanned in to the inhibit signal on a NIM gate and delay card. The diagrams below show common deadtime operation with external trigger and flow control. The diagram on the right shows how to synchronise a SAC module and a VME ADC in the same system.



GRT4 System Diagram



GRT4 plus 9418 & SAC System Diagram

The GRT4 card will ignore any further triggers which occur while it is processing a trigger (except for using them to detect pileup). The Inhibit/Busy output is driven whilst a trigger is being processed and cleared when the data are written to the output buffer. When any channel of the GRT4 fills its output buffer the card will continue to drive its Inhibit/Busy output until the buffer has been read and space for data is again available.

Where flow control is not required, the front panel trigger out can be used. Under the control of the ADC Trigger register the output can be programmed to either retransmit the front panel trigger input or else to OR in the triggers generated by the CFDs in this GRT4 card. Care should be taken about the propagation delays when daisy chaining cards together.

5 Jumpers:

All orientations are given looking at component side of PCB, with VME 96 way connectors on right.

Switches are labelled ON with an arrow to indicate which is ON and which is OFF.

5.1 Input differentiation on/off:

Channel A: SW1 open = differentiate; closed = no differentiation.
Channel B: SW2 open = differentiate; closed = no differentiation.
Channel C: SW3 open = differentiate; closed = no differentiation.
Channel D: SW4 open = differentiate; closed = no differentiation.

5.2 Mode lines for reprogrammable (DPP) LCAs.

Channel	Jumpers	For PROM loading (mode 000)	For JTAG loading (mode 101)
A	PS16,PS17	Connect pins 2-3 only	Connect pins 1-2 only
B	PS19, PS20	Connect pins 2-3 only	Connect pins 1-2 only
C	PS22, PS23	Connect pins 2-3 only	Connect pins 1-2 only
D	PS25, PS26	Connect pins 2-3 only	Connect pins 1-2 only

NB Pin 1 is the top pin on all these jumpers

5.3 DPP LCA JTAG Reprogramming inputs:

Normally open circuit.
To reprogram, set mode line jumpers (5.2) to JTAG and connect Xilinx JTAG programming lead to:
JT1 for channel A
JT3 for channel B
JT2 for channel C
JT4 for channel D
(NB not quite in sequence)

5.4 LCA Reprogram inputs:

Switches set to off normally (turn ON and back to OFF to reload the LCA)
VME LCA: PS14
Channel A: ADC LCA reloaded by PS10; DPP LCA reloaded by PS15
Channel B: ADC LCA reloaded by PS11; DPP LCA reloaded by PS21
Channel C: ADC LCA reloaded by PS12; DPP LCA reloaded by PS18
Channel D: ADC LCA reloaded by PS13; DPP LCA reloaded by PS24

5.5 Master reset for whole card:

Normally OFF; turn ON to reset, then OFF to allow normal operation; PS9

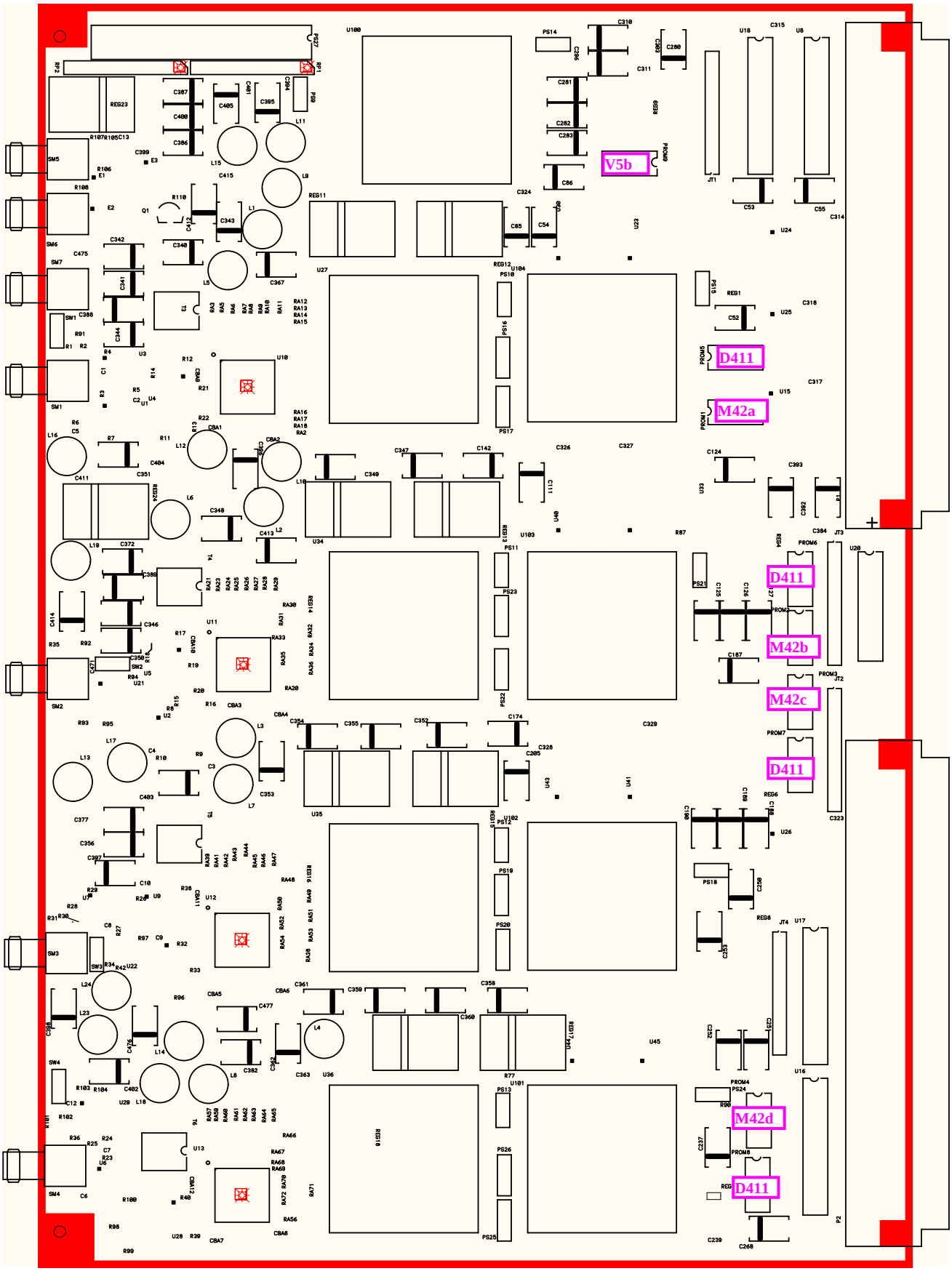
5.6 VME Base address

The VME base address is set using the switches at PS27.

The left switch is the LSB (A16), the right is MSB (A31).

Switches ON (up) are 0, switches OFF (down) are 1.

6 Board Layout



7 LCA versions and PROM signal names:

In Aug 2006 the latest PROM versions are 4.2 for ADC, 4.11 for DPP and P5B for VME.

Use of "spare" signals:
Common_Sp0 = SysReset
Common_Sp1 = Trigger in
Common_Sp2 = Gate in
Common_Sp3 = Trigger Out (driven from channel D only)
Common_Sp4 = Trig_A
Common_Sp5 = Trig_B
Common_Sp6 = Trig_C
Common_Sp7 = Trig_D
Common_Sp8 = Data Strobe
Common_Sp9 = common_clock
Common_Sp10 = enable decoded addressing (from VME LCA)
Common_Sp11-18 = Address for decoded VME addressing (from VME LCA)
Common_sp19-23 = unused

ADC_DPP_SP0= "Cycle" from DPP LCA to ADC LCA (instead of "my cycle" on ADC lca pin 120)
ADC_DPP_SP1= "Read Header" from DPP LCA to ADC LCA (non ADC data including timestamp)
ADC_DPP_SP2= "Enable_ADC_Read" from DPP LCA to ADC LCA (read ADC data buffer)
ADC_DPP_SP3= "Soft Reset" from ADC LCA to DPP LCA
ADC_DPP_SP4= "Trig" (requested triggers) from ADC LCA to DPP LCA
ADC_DPP_SP5-8= MWD Address for readout of blr, energy etc. from DPP LCA to ADC LCA
ADC_DPP_SP9 = dpp_read_mwd from DPP LCA to ADC LCA
ADC_DPP_SP10 = dpp_strobe_mwd from DPP LCA to ADC LCA
ADC_DPP_SP11 = my_ready (MWD data ready) from ADC LCA to DPP LCA

DPPv3 and later depends on ADC_buf_v2 or later (both dated 19th August 2002) because the ADC_DPP_SP3 line is used as soft reset from ADC LCA to DPP LCA- if floating it will look like a reset.