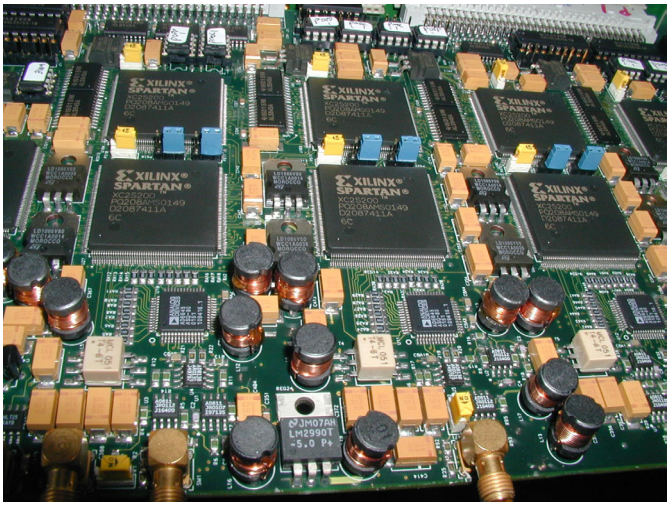
Daresbury GRT4 (Gamma Ray Tracking 4 Channel) VME Module

Overview



The Daresbury GRT4 VME module is designed to do digital pulse processing for gamma ray tracking. It includes four acquisition channels operating in parallel. Each channel has a 14 bit 80MHz flash ADC[1]. The processing and data buffering is performed by two dedicated Xilinx Spartan 2 FPGAs per channel. Each FPGA has 200k gates available. The first contains a circular buffer (256 or 512 samples deep) with programmable pretrigger delay and a digital trigger. Each trace in this buffer is tagged with a 16 bit header (8 ID bits are programmable, 8 bits are the trigger counter) and a 48 bit timestamp when the trigger occurs. The second is intended for pulse processing (such as MWD energy algorithm[2], timing or interaction position). In its simplest form it can be used as a 2k x 16 data buffer for readout of raw pulse traces. The analogue inputs are filtered with a 40MHz low pass filter and include an optional differentiation stage so that the ADC is presented with either the raw input or a differentiated input representing the detector current pulse.

In addition to each channel's digital triggering, there is an external trigger input (one per card, distributed to all 4 channels) and a trigger output. This permits an external trigger to be propagated down several GRT VME cards using a daisy chain or a parallel connection. As well as trigger in/out there is a gate (inhibit) input which synchronises multiple modules, for example making them all dead during readout of pulse traces. Each channel of the card can either observe the trigger input and propagate it or else it can modify it by making a logic OR of its own trigger detection with the incoming trigger. It is therefore possible to trigger adjacent channels to look for low level induced charge which might be too small to trigger them otherwise.

Specification

Analogue Inputs: 4 SMA connectors

- **In non-differentiated configuration:**
  0 to ±550mV at input (i.e. 1.1V unterminated) input range
  Maximum input represents 5.5MeV for typical 200mV/MeV preamplifier sensitivity and no baseline shift.
- **In differentiated configuration:**
  ±15mV/ns at the input (i.e. 30mV/ns unterminated) is converted to the ADC's full scale value
  This equates to a 7.5MeV input (200mV/MeV sensitivity) switching in 50ns.

Trigger Inputs/Outputs: 3 SMA Connectors

- Trigger In (Fast NIM)
- Busy Output (can alternatively be used as a Trigger Out under software control) (Fast NIM)
- Gate In (Fast NIM)

ADC:

- 14 bits 80 MHz. (Bipolar inputs generating 2's complement data)
- Typical DNL = ±0.25LSB,
- Typical INL= ±0.5LSB

Maximum Data Rate:
Maximum readout rate is about 6Mbyte/second for the whole module using block transfers to an MVME2431 PowerPC processor. It is difficult to equate this to input counting rate because the number of parameters read will vary depending on the processing. If the card produces a header word, 3 timestamp words and 4 parameter words for each trace then the maximum input counting rate would be 750kHz shared across all 4 channels. However if the raw data traces are read then the counting rate drops to about 12kHz shared across all 4 channels.

Status: The first production run took place in July 2002 for the UK's Gamma Ray Tracking Project. A MIDAS user interface exists to control the GRT4 cards and collect data to tape. In February 2003 a 64 channel system was used in an experiment.

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[1] A pin compatible 105MHz 14bit ADC will be available during 2002 and will be used for any further production runs.
[2] "An analog-to-digital conversion based on a moving window deconvolution" Authors: Georgiev, Gast and Lieder
IEEE TNS Volume: 41 Issue: 4 Part: 1-2 , Aug. 1994 Page(s): 1116 -1124

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Issue 2a March 2003

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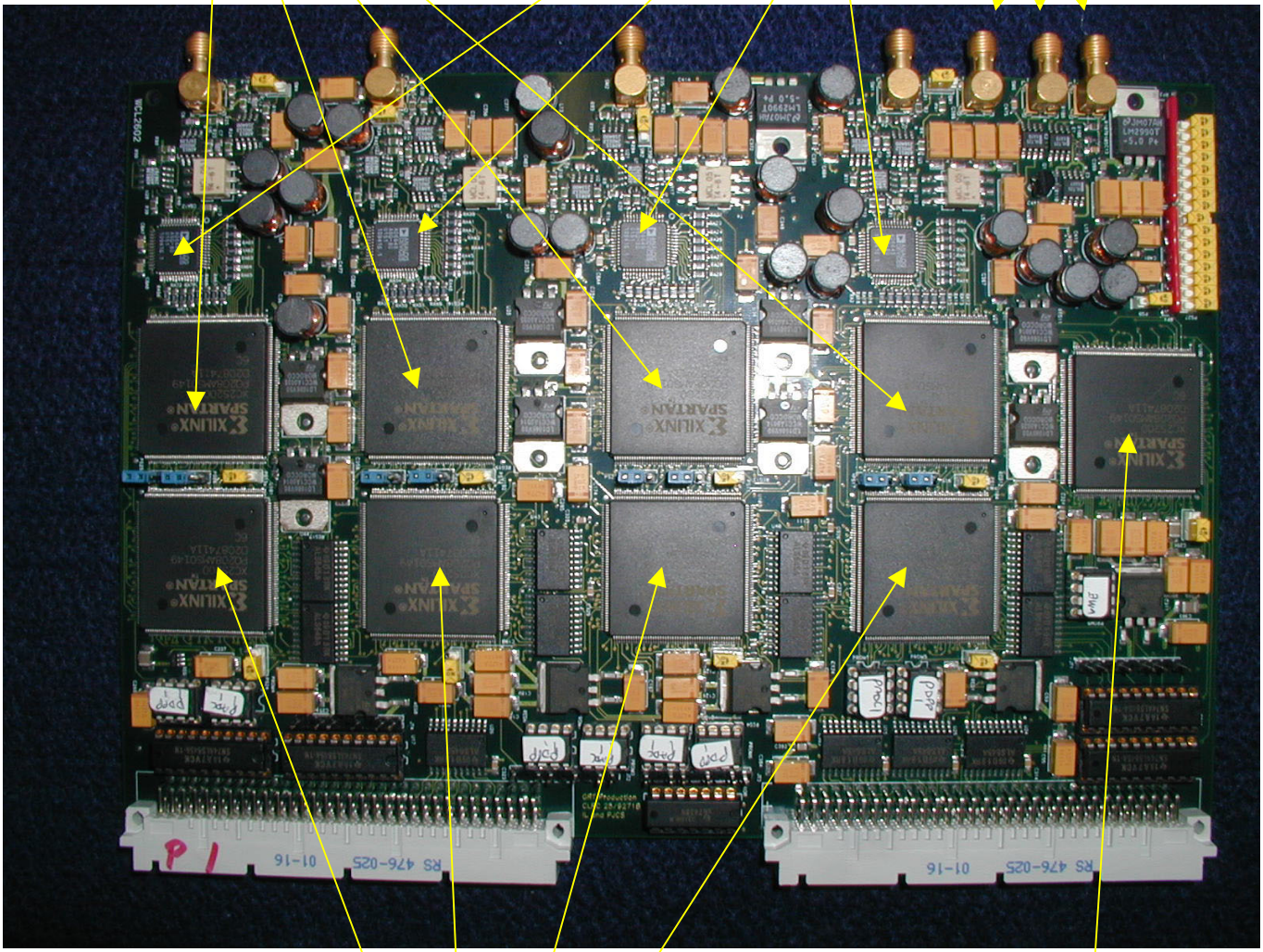
ADC Control, triggering and circular buffer in Xilinx FPGAs

14 bits 80MHz ADC type AD6645

Trigger in, gate in and trigger out (all SMA)



Xilinx FPGAs for processing data traces. 200k gate Spartan 2 device per channel.

VME Interface control and decode

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