AGATA digitiser internal connector cross reference V3

ADC segment card to Power card connectors

IN Refers to signals INTO the FADC card

Signal name	No of wires	Signal type	Connector		Source of signal	Destination of signal	A	B	C
SYNC IN	2	LVDS	A		CORE DRIVER/VIRTEX	SYNC RECEIVER	2	0	0
SLOW CONTROL IN CLK	2	LVDS	B		SPARTAN	VIRTEX	0	2	0
SLOW CONTROL IN DATA	2	LVDS	B		SPARTAN	VIRTEX	0	2	0
SLOW CONTROL IN FRAME	1	LVCMOS25	B		SPARTAN	VIRTEX	0	1	0
SLOW CONTROL OUT CLK	2	LVDS	B		VIRTEX	SPARTAN	0	2	0
SLOW CONTROL OUT DATA	2	LVDS	B		VIRTEX	SPARTAN	0	2	0
SLOW CONTROL OUT FRAME	1	LVCMOS25	B		VIRTEX	SPARTAN	0	1	0
I/O RESET OUT/IN	1	OPEN DRAIN LVCMOS25	B		SPARTAN (COMMON)	VIRTEX (COMMON)	0	1	0
TEMPERATURE MONITOR SELECT IN	2	LVTTL	B		SPARTAN	TEMPERATURE CHIPS	0	2	0
TEMPERATURE MONITOR DATA OUT	1	LVTTL	B		TEMPERATURE CHIPS	SPARTAN	0	1	0
TEMPERATURE MONITOR CLOCK IN	1	LVTTL	B		SPARTAN	TEMPERATURE CHIPS	0	1	0
GENERAL RESET IN	1	OPEN DRAIN LVCMOS25	C		SPARTAN	VIRTEX	0	0	1
MODE IN	3	LVCMOS25	C		SPARTAN	VIRTEX	0	0	3
VIRTEX PROGRAMMING GEN IN/OUT	15	LVCMOS25	B/C		VIRTEX/SPARTAN	VIRTEX/SPARTAN	0	10	5
VIRTEX PROGRAMMING PROG IN/OUT	1	OPEN DRAIN LVCMOS25	C		VIRTEX/SPARTAN	VIRTEX/SPARTAN	0	0	1
CLOCK ENABLE IN	1	OPEN DRAIN LVCMOS25	A		SPARTAN	CLOCK RECEIVER	1	0	0
SPARE LINES	6	LVCMOS25	B		SPARTAN	VIRTEX AND PADS ON PCB	0	6	0
POWER 1.5V/1A FPGA IN	4	POWER	C		POWER	VIRTEX CORE	0	0	4
POWER 2.5V/1A FPGA IN	4	POWER	C		POWER	VIRTEX I/O	0	0	4
POWER 3.3V/2A FPGA/LASER IN	6	POWER	C		POWER	LASER/VIRTEX LASER I/O	0	0	6
POWER 3.3V/<2A FPGA I/O IN	6	POWER	C		POWER	VIRTEX I/O	0	0	6
POWER 3.3V/1A CLOCK DISTRIB IN	4	POWER	A		POWER	CLOCK RECEIVER ETC.	4	0	0
POWER 6.5V/<2.5A ANALOGUE IN	6	POWER	A		POWER	ANALOGUE REGULATOR	6	0	0
POWER -6.5V/1A ANALOGUE IN	4	POWER	A		POWER	ANALOGUE REGULATOR	4	0	0
POWER 12V/0.5A RELAYS IN	2	POWER	A		POWER	RELAYS	2	0	0
GROUND FOR CONNECTOR A	28	GROUND	A		GND	ANALOGUE GROUND RET	28	0	0
GROUND FOR CONNECTOR B	19	GROUND	B		GND	DIGITAL GROUND RET	0	19	0
GROUND FOR CONNECTOR C	20	GROUND	C		GND	DIGITAL GROUND RET	0	0	20
ISOLATED +5V/-5V/0V	3	POWER/GROUND	A		BACKPLANE CONNECTOR	PREAMP ISOLATORS	3	0	0

TOTAL PINS	150	50	50	50
PINS PER CONNECTOR	50			

ADC CORE card to Power card connectors

IN Refers to signals INTO the FADC card

Signal name	No of wires	Signal type	Connector		Source of signal	Destination of signal	A	B	C
RESYNC OUT (main sync from C virtex)	2	LVDS	A		SYNC VIRTEX	SYNC DRIVER	2	0	0
SYNC IN	2	LVDS	A		SYNC DRIVER	ALL VIRTEX	2	0	0
SLOW CONTROL IN CLK	2	LVDS	B		SPARTAN	VIRTEX	0	2	0
SLOW CONTROL IN DATA	2	LVDS	B		SPARTAN	VIRTEX	0	2	0
SLOW CONTROL IN FRAME	1	LVCMOS25	B		SPARTAN	VIRTEX	0	1	0
SLOW CONTROL OUT CLK	2	LVDS	B		VIRTEX	SPARTAN	0	2	0
SLOW CONTROL OUT DATA	2	LVDS	B		VIRTEX	SPARTAN	0	2	0
SLOW CONTROL OUT FRAME	1	LVCMOS25	B		VIRTEX	SPARTAN	0	1	0
I/O RESET OUT/IN	1	OPEN DRAIN LVCMOS25	B		SPARTAN (COMMON)	VIRTEX	0	1	0
TEMPERATURE MONITOR SELECT IN	2	LVTTL	B		SPARTAN	TEMPERATURE CHIPS	0	2	0
TEMPERATURE MONITOR DATA OUT	1	LVTTL	B		TEMPERATURE CHIPS	SPARTAN	0	1	0
TEMPERATURE MONITOR CLOCK IN	1	LVTTL	B		SPARTAN	TEMPERATURE CHIPS	0	1	0
GENERAL RESET IN	1	OPEN DRAIN LVCMOS25	B		SPARTAN	VIRTEX	0	0	1
MODE IN	3	LVCMOS25	C		SPARTAN	VIRTEX	0	0	3
VIRTEX PROGRAMMING GEN IN/OUT	15	LVCMOS25	B/C		VIRTEX/SPARTAN	VIRTEX/SPARTAN	0	10	5
VIRTEX PROGRAMMING PROG IN/OUT	1	OPEN DRAIN LVCMOS25	C		VIRTEX/SPARTAN	VIRTEX/SPARTAN	0	0	1
CLOCK ENABLE IN	1	OPEN DRAIN LVCMOS25	A		SPARTAN	CLOCK RECEIVER	1	0	0
CLOCK SOURCE SELECT IN	1	LVCMOS25	C		SPARTAN	CRYSTAL/CLK SEL CHIP	0	0	1
SPARE LINES	6	LVCMOS25	B		SPARTAN	VIRTEX AND PADS ON PCB	0	6	0
POWER 1.5V/1A FPGA IN	4	POWER	C		POWER	VIRTEX CORE	0	0	4
POWER 2.5V/1A FPGA IN	4	POWER	C		POWER	VIRTEX I/O	0	0	4
POWER 3.3V/2A FPGA/LASER IN	6	POWER	B		POWER	LASER/VIRTEX LASER I/O	0	0	6
POWER 3.3V/<2A FPGA I/O IN	6	POWER	B		POWER	VIRTEX I/O	0	0	6
POWER 3.3V/1A CLOCK DISTRIB IN	4	POWER	A		POWER	CLOCK RECEIVER ETC.	4	0	0
POWER 6.5V/<2.5A ANALOGUE IN	6	POWER	A		POWER	ANALOGUE REGULATOR	6	0	0
POWER -6.5V/1A ANALOGUE IN	4	POWER	A		POWER	ANALOGUE REGULATOR	4	0	0
POWER 12V/0.5A RELAYS/RF/PLL IN	2	POWER	A		POWER	RF POWER AMP/RELAYS	2	0	0
GROUND FOR CONNECTOR A	26	GROUND	A		GND	ANALOGUE GROUND RET	26	0	0
GROUND FOR CONNECTOR B	19	GROUND	B		GND	DIGITAL GROUND RET	0	19	0
GROUND FOR CONNECTOR C	19	GROUND	C		GND	DIGITAL GROUND RET	0	0	19
ISOLATED +5V/-5V/0V	3		A		BACKPLANE CONNECTOR	PREAMP ISOLATORS	3	0	0

TOTAL PINS	150
PINS PER CONNECTOR	50

50	50	50

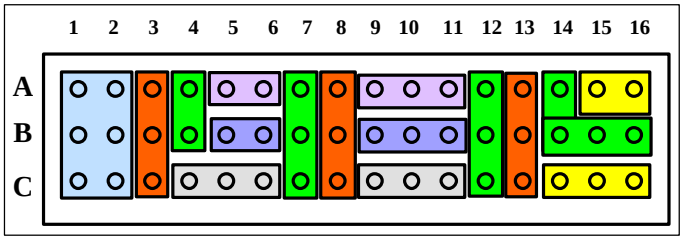
BACKPLANE to Segment Power card connectors

IN Refers to signals INTO the Power card card

Signal name	No of wires	Signal type	Connector Allocation	Source of signal	Destination of signal
isolated +5V/-5V/0V supply IN	6	power supply	A1/2,C1/2,B1/2	External 9 pin D connector	SEGMENT ADC ISOLATORS
Main +12V/15A MAX supply feed	9	power supply	A3/8/13,B3/8/13, C3/8/13	POWER	POWER
Main 0V ground return	12	power supply / signal return	A4/7/12/14,B4/7/12/14/15/16,C7/12	POWER	POWER
SYNC IN	2	LVDS	A15,A16	SYNC DRIVER	FADC SYNC RECEIVER
SLOW CONTROL OUT CLK	2	LVDS	A5,A6	CORE SPARTAN	SEGMENT SPARTAN
SLOW CONTROL OUT DATA	2	LVDS	A10,A11	CORE SPARTAN	SEGMENT SPARTAN
SLOW CONTROL OUT FRAME	1	LVCMOS25	A9	CORE SPARTAN	SEGMENT SPARTAN
SLOW CONTROL IN CLK	2	LVDS	B5,B6	SEGMENT SPARTAN	CORE SPARTAN
SLOW CONTROL IN DATA	2	LVDS	B10,B11	SEGMENT SPARTAN	CORE SPARTAN
SLOW CONTROL IN FRAME	1	LVCMOS25	B9	SEGMENT SPARTAN	CORE SPARTAN
I/O RESET OUT/IN	1	OPEN DRAIN LVCMOS25	C14	SPARTAN/VIRTEX	SPARTAN/VIRTEX
GENERAL RESET IN	1	OPEN DRAIN LVCMOS25	C15	CORE SPARTAN	SEGMENT SPARTAN
SEGMENT POWER SUPPLY OK OUT	1	LVCMOS25	C16	SEGMENT SPARTAN	CORE SPARTAN
SPARE LINES	6	LVCMOS25	C4/5/6/9/10/11	SPARTAN/VIRTEX	SPARTAN/VIRTEX

TOTAL SIGNALS	48

A2,B2,C2 MAY BE USED FOR +12V



NOTES
ALL SPARE SIGNALS ENTER BOARDS AFTER PASSING THROUGH ZERO OHM LINKS ON POWER BOARD SO THAT THEY MAY BE CONNECTED IF REQUIRED.

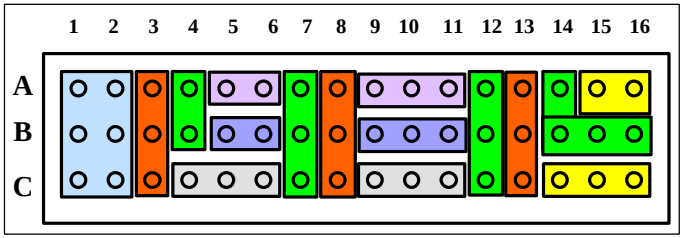
BACKPLANE to Core Power card connectors

IN Refers to signals INTO the Power card card

Signal name	No of wires	Signal type	Connector Allocation	Source of signal	Destination of signal
isolated +5V/-5V/0V supply IN	6	power supply	A1/2,C1/2,B1/2	External 9 pin D connector	CORE ADC ISOLATORS
Main +12V supply feed OUT	10	power supply	A3/8/13,B3/8/13, C3/8/13	POWER	POWER
Main 0V ground return	11	power supply / signal return	A4/7/12/14,B4/7/12/14/15/16,C7/12	POWER	POWER
SYNC OUT	2	LVDS	A15,A16	SYNC DRIVER	FADC SYNC RECEIVERS
SLOW CONTROL IN CLK	2	LVDS	A5,A6	SEGMENT SPARTAN	CORE SPARTAN
SLOW CONTROL IN DATA	2	LVDS	A10,A11	SEGMENT SPARTAN	CORE SPARTAN
SLOW CONTROL IN FRAME	1	LVCMOS25	A9	SEGMENT SPARTAN	CORE SPARTAN
SLOW CONTROL OUT CLK	2	LVDS	B5,B6	CORE SPARTAN	SEGMENT SPARTAN
SLOW CONTROL OUT DATA	2	LVDS	B10,B11	CORE SPARTAN	SEGMENT SPARTAN
SLOW CONTROL OUT FRAME	1	LVCMOS25	B9	CORE SPARTAN	SEGMENT SPARTAN
I/O RESET OUT/IN	1	OPEN DRAIN LVCMOS25	C14	SPARTAN/VIRTEX	SPARTAN/VIRTEX
GENERAL RESET OUT	1	OPEN DRAIN LVCMOS25	C15	CORE SPARTAN	SEGMENT SPARTAN
SEGMENT POWER SUPPLY OK IN	1	LVCMOS25	C16	SEGMENT SPARTAN	CORE SPARTAN
SPARE LINES	6	LVCMOS25	C4/5/6/9/10/11	SPARTAN/VIRTEX	SPARTAN/VIRTEX

TOTAL SIGNALS	48

A2,B2,C2 MAY BE USED FOR +12V



NOTES
ALL SPARE SIGNALS ENTER BOARDS AFTER PASSING THROUGH ZERO OHM LINKS ON POWER BOARD SO THAT THEY MAY BE CONNECTED IF REQUIRED.

Control card to Power card connectors

IN Refers to signals INTO the control card

Signal name	No of wires	Signal type *(Core)*	Connector		Source of signal	Destination of signal	A	B	C
SLOW CONTROL CORE (1 IN/1 OUT)	2	LVCMOS25	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	2
SLOW CONTROL CORE (2 IN/2 OUT)	8	LVDS	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	8
SLOW CONTROL VIRT 1 (1 IN/1 OUT)	2	LVCMOS25	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	2
SLOW CONTROL VIRT 1 (2 IN/2 OUT)	8	LVDS	A		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	8	0	0
SLOW CONTROL VIRT 2 (1 IN/1 OUT)	2	LVCMOS25	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	2
SLOW CONTROL VIRT 2 (2 IN/2 OUT)	8	LVDS	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	8
SLOW CONTROL VIRT 3 (1 IN/1 OUT)	2	LVCMOS25	C		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	0	0	2
SLOW CONTROL VIRT 3 (2 IN/2 OUT)	8	LVDS	A		CONTROL SPARTAN I/O	CONTROL SPARTAN I/O	8	0	0
**SLOW CONTROL VIRT 4 (1 IN/1 OUT)*	*2*	*LVCMOS25 (clksel, pwr OK in)*	*B*		*CONTROL SPARTAN I/O*	*CONTROL SPARTAN I/O*	0	2	0
SLOW CONTROL VIRT 4 (2 IN/2 OUT)	*8*	*LVDS*	*B*		*CONTROL SPARTAN I/O*	*CONTROL SPARTAN I/O*	0	8	0
VIRTEX PROGRAM COMMON	11	LVCMOS25 OR OPEN DRAIN	B		CONTROL SPARTAN	ALL MODULE VIRTEX	0	11	0
VIRTEX PROGRAM CONFIG 1	8	LVCMOS25	B		CONTROL SPARTAN	FADC VIRTEX 1	0	8	0
VIRTEX PROGRAM CONFIG 2	8	LVCMOS25	B		CONTROL SPARTAN	FADC VIRTEX 2	0	8	0
VIRTEX PROGRAM CONFIG 3	8	LVCMOS25	C		CONTROL SPARTAN	FADC VIRTEX 3	0	0	8
** VIRTEX PROGRAM CONFIG 4*	*8*	*LVCMOS25 (power off out)*	*C*		*CONTROL SPARTAN*	*FADC VIRTEX 4 (FIAM)*	0	0	8
100MHZ ADC CLOCK ENABLE OUT	1	O/D LVCMOS25/LVTTL (MOD)	A		CONTROL SPARTAN	ALL MODULE CLOCK RX	1	0	0
COMMS RESET (O/C) FULL BOX	1	OPEN DRAIN LVCMOS25	A		COMMON O/C I/O TO ALL	COMMON O/C I/O TO ALL	1	0	0
GENERAL RESET (REGISTERS)(O/C)	1	OPEN DRAIN LVCMOS25	B		EITHER SPARTAN	ALL VIRTEX AND SPARTAN	0	1	0
TEMP MON CS0/1	10	LVTTL	A		CONTROL SPARTAN	TEMP MONITOR CHIPS	10	0	0
TEMP MON DATA AND CLOCK	2	LVTTL	A		CONTROL SPARTAN	TEMP MONITOR CHIPS	2	0	0
* SPARES 1 *	4	LVCMOS25	A		CONTROL SPARTAN I/O	ALL VIRTEX AND SPARTAN	4	0	0
* SPARES 2 *	2	LVCMOS25	C		CONTROL SPARTAN I/O	ALL VIRTEX AND SPARTAN	0	0	2
3.3V DC	4	POWER	A		POWER BOARD	CONTROL BOARD	4	0	0
2.5V DC	4	POWER	A		POWER BOARD	CONTROL BOARD	4	0	0
1.2V DC monitor	1	POWER	A		POWER BOARD	CONTROL BOARD	1	0	0
SEGMENT POWER OK	1	LVCMOS25	C		SEGMENT POWER	BOTH CONTROL SPARTAN	0	0	1
GROUND A	6	GROUND	A		POWER BOARD	CONTROL BOARD	6	0	0
GROUND B	12	GROUND	B		POWER BOARD	CONTROL BOARD	0	12	0
GROUND C	7	GROUND	C		POWER BOARD	CONTROL BOARD	0	0	7

TOTAL PINS	149
PINS PER CONNECTOR	50

Signals in Italics are not present or required on the CORE control card and may have a second use

49	50	50

* VIRTEX PROGRAM CONFIG 4 in CORE is used as POWER OFF and SLOW CONTROL VIRT 4 used for CLOCK SELECT and CORE POWER OK

* SPARE Signals are undefined LVCMOS25 or LVDS and can connect any programmable device(s) to any other(s) in the BOX

SEGMENT POWER to ADC card connector A connections

	Connector A			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	GND	1	2	GND
	GND	3	4	GND
	Analogue +6V5	5	6	Analogue +6V5
	Analogue +6V5	7	8	Analogue +6V5
	Analogue +6V5	9	10	Analogue +6V5
	GND	11	12	GND
	GND	13	14	GND
	GND	15	16	GND
	Analogue -6V5	17	18	Analogue -6V5
	Analogue -6V5	19	20	Analogue -6V5
	GND	21	22	GND
	GND	23	24	GND
	Relays +12V	25	26	Relays +12V
	GND	27	28	GND
	GND	29	30	GND
	CLK Sync +LVDS	31	32	CLK Sync -LVDS
	GND	33	34	GND
	GND	35	36	GND
	GND	37	38	GND
	CLK Power 3V3	39	40	CLK Power 3V3
	CLK Power 3V3	41	42	CLK Power 3V3
	GND	43	44	GND
	GND	45	46	GND
	CLK_Enable	47	48	0V Isolated
To Front of Module	-5V Isolated	49	50	+5V Isolated

SEGMENT POWER to ADC card connector B connections

	Connector B			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	Spare1	1	2	Spare2
	GND	3	4	GND
	GND	5	6	GND
	Spare3	7	8	Spare4
	Spare5	9	10	Spare6
	GND	11	12	GND
	GND	13	14	GND
	D7	15	16	D6
	D5	17	18	D4
	D3	19	20	D2
	GND	21	22	GND
	D1	23	24	D0
	RDWR_B	25	26	Busy
	GND	27	28	GND
	SC_Clock_in+	29	30	SC_Clock_in-
	SC_Data_in+	31	32	SC_Data_in-
	SC_Frame_in	33	34	GND
	GND	35	36	SC_Frame_out
	SC_Data_out+	37	38	SC_Data_out-
	SC_Clock_out+	39	40	SC_Clock_out-
	GND	41	42	GND
	Temperature Select0	43	44	Temperature Select1
	GND	45	46	GND
	Temperature Clock	47	48	Temperature Data
To Front of Module	I/O reset	49	50	GND

SEGMENT POWER to ADC card connector C connections

	Connector C			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	GND	1	2	GND
	Laser Power 3.3Volts	3	4	Laser Power 3.3Volts
	Laser Power 3.3Volts	5	6	Laser Power 3.3Volts
	Laser Power 3.3Volts	7	8	Laser Power 3.3Volts
	GND	9	10	GND
	GND	11	12	GND
	VCCIO 3.3Volts	13	14	VCCIO 3.3Volts
	VCCIO 3.3Volts	15	16	VCCIO 3.3Volts
	VCCIO 3.3Volts	17	18	VCCIO 3.3Volts
	GND	19	20	GND
	GND	21	22	GND
	Mode0	23	24	Mode1
	Mode2	25	26	INIT
	PROG	27	28	CCLK
	DONE	29	30	CS_B_V
	General Reset	31	32	Echo_Done
	GND	33	34	GND
	VCCINT 1.5 volts	35	36	VCCINT 1.5 volts
	VCCINT 1.5 volts	37	38	VCCINT 1.5 volts
	GND	39	40	GND
	GND	41	42	GND
	VCCAUX 2.5 volts	43	44	VCCAUX 2.5 volts
	VCCAUX 2.5 volts	45	46	VCCAUX 2.5 volts
	GND	47	48	GND
To Front of Module	GND	49	50	GND

CORE POWER to ADC card connector A connections

	Connector A			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	RESYNC IN+	1	2	RESYNC IN-
	GND	3	4	GND
	Analogue +6V5	5	6	Analogue +6V5
	Analogue +6V5	7	8	Analogue +6V5
	Analogue +6V5	9	10	Analogue +6V5
	GND	11	12	GND
	GND	13	14	GND
	GND	15	16	GND
	Analogue -6V5	17	18	Analogue -6V5
	Analogue -6V5	19	20	Analogue -6V5
	GND	21	22	GND
	GND	23	24	GND
	Relays +12V	25	26	Relays +12V
	GND	27	28	GND
	GND	29	30	GND
	CLK Sync +LVDS	31	32	CLK Sync -LVDS
	GND	33	34	GND
	GND	35	36	GND
	GND	37	38	GND
	CLK Power 3V3	39	40	CLK Power 3V3
	CLK Power 3V3	41	42	CLK Power 3V3
	GND	43	44	GND
	GND	45	46	GND
	CLK_Enable	47	48	0V Isolated
To Front of Module	-5V Isolated	49	50	+5V Isolated

CORE POWER to ADC card connector B connections

	Connector B			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	Spare1	1	2	Spare2
	GND	3	4	GND
	GND	5	6	GND
	Spare3	7	8	Spare4
	Spare5	9	10	Spare6
	GND	11	12	GND
	GND	13	14	GND
	D7	15	16	D6
	D5	17	18	D4
	D3	19	20	D2
	GND	21	22	GND
	D1	23	24	D0
	RDWR_B	25	26	Busy
	GND	27	28	GND
	SC_Clock_in+	29	30	SC_Clock_in-
	SC_Data_in+	31	32	SC_Data_in-
	SC_Frame_in	33	34	GND
	GND	35	36	SC_Frame_out
	SC_Data_out+	37	38	SC_Data_out-
	SC_Clock_out+	39	40	SC_Clock_out-
	GND	41	42	GND
	Temperature Select0	43	44	Temperature Select1
	GND	45	46	GND
	Temperature Clock	47	48	Temperature Data
To Front of Module	I/O reset	49	50	GND

CORE POWER to ADC card connector C connections

	Connector C			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	GND	1	2	GND
	Laser Power 3.3Volts	3	4	Laser Power 3.3Volts
	Laser Power 3.3Volts	5	6	Laser Power 3.3Volts
	Laser Power 3.3Volts	7	8	Laser Power 3.3Volts
	GND	9	10	GND
	GND	11	12	GND
	VCCIO 3.3Volts	13	14	VCCIO 3.3Volts
	VCCIO 3.3Volts	15	16	VCCIO 3.3Volts
	VCCIO 3.3Volts	17	18	VCCIO 3.3Volts
	GND	19	20	GND
	GND	21	22	GND
	Mode0	23	24	Mode1
	Mode2	25	26	INIT
	PROG	27	28	CCLK
	DONE	29	30	CS_B_V
	General Reset	31	32	Echo_Done
	GND	33	34	GND
	VCCINT 1.5 volts	35	36	VCCINT 1.5 volts
	VCCINT 1.5 volts	37	38	VCCINT 1.5 volts
	GND	39	40	GND
	GND	41	42	GND
	VCCAUX 2.5 volts	43	44	VCCAUX 2.5 volts
	VCCAUX 2.5 volts	45	46	VCCAUX 2.5 volts
	GND	47	48	GND
To Front of Module	CLK Source Select	49	50	GND

CORE POWER to CONTROL card connector A connections

	Connector A			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	V1 SC_Clock_in+	1	2	V1 SC_Clock_in-
	V1 SC_Data_in+	3	4	V1 SC_Data_in-
	V1 SC_Data_out+	5	6	V1 SC_Data_out-
	V1 SC_Clock_out+	7	8	V1 SC_Clock_out-
	V2 SC_Clock_in+	9	10	V2 SC_Clock_in-
	V2 SC_Data_in+	11	12	V2 SC_Data_in-
	V2 SC_Clock_out+	13	14	V2 SC_Clock_out-
	V2 SC_Data_out+	15	16	V2 SC_Data_out-
	SPARE 1 (LVDS/LVCMOS)	17	18	SPARE 2 (LVDS/LVCMOS)
	SPARE 3 (LVDS/LVCMOS)	19	20	SPARE 4 (LVDS/LVCMOS)
	GND	21	22	GND
	V1 TEMP EN 0	23	24	V1 TEMP EN 1
	V2 TEMP EN 0	25	26	V2 TEMP EN 1
	(CORE) V3 TEMP EN 0	27	28	V3 TEMP EN 1 (CORE)
	P/S TEMP EN 2	29	30	*SPARE LVTTL PIN*
	P/S TEMP EN 0	31	32	P/S TEMP EN 1
	TEMP DATA	33	34	TEMP CLK
	GND	35	36	GND
	COMMS RESET	37	38	VIRTEX CLOCK ENABLE
	VCC IO 3.3Volts	39	40	VCC IO 3.3Volts
	VCC IO 3.3Volts	41	42	VCC IO 3.3Volts
	VCC IO 2.5Volts	43	44	VCC IO 2.5Volts
	VCC IO 2.5Volts	45	46	VCC IO 2.5Volts
	GND	47	48	GND
To Front of Module	NOT CONNECTED	49	50	VCCINT 1.8V MONITOR

CORE POWER to CONTROL card connector B connections

To Rear of Module

Connector B			
Signal name	**Pin**	**Pin**	**Signal name**
LVDS/LVCMOS25 SPARE	1	2	*LVDS/LVCMOS25 SPARE*
LVDS/LVCMOS25 SPARE	3	4	*LVDS/LVCMOS25 SPARE*
LVDS/LVCMOS25 SPARE	5	6	*LVDS/LVCMOS25 SPARE*
LVDS/LVCMOS25 SPARE	7	8	*LVDS/LVCMOS25 SPARE*
CLOCK SOURCE SEL	9	10	CORE POWER OK IN
GND	11	12	GND
V1 BUSY	13	14	V1 PROG
V1 INIT	15	16	V1 DONE
V1 CS_B	17	18	V1 ECHO DONE
V1 CCLK	19	20	V1 D0
GND	21	22	GND
V2 BUSY	23	24	V2 PROG
V2 INIT	25	26	V2 DONE
V2 CS_B	27	28	V2 ECHO DONE
V2 CCLK	29	30	V2 D0
GND	31	32	GND
MODE 0	33	34	MODE 1
MODE 2	35	36	RDWR_B
GND	37	38	GND
D1	39	40	D2
D3	41	42	D4
D5	43	44	D6
D7	45	46	GND
GND	47	48	GND
GND	49	50	GENERAL RESET

To Front of Module

CORE POWER to CONTROL card connector C connections

	Connector C			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	SEG/CORE SC_Clock_in+	1	2	SEG/CORE SC_Clock_in-
	SEG/CORE SC_Data_in+	3	4	SEG/CORE SC_Data_in-
	SEG/CORE SC_Data_out+	5	6	SEG/CORE SC_Data_out-
	SEG/CORE SC_Clock_out+	7	8	SEG/CORE SC_Clock_out-
	SEG/CORE FRAME IN	9	10	SEG/CORE FRAME OUT
	GND	11	12	SEGMENT POWER OK IN
	V2 FRAME IN	13	14	V2 FRAME OUT
	V3 SC_Clock_in+	15	16	V3 SC_Clock_in-
	V3 SC_Data_in+	17	18	V3 SC_Data_in-
	V3 SC_Data_out+	19	20	V3 SC_Data_out-
	V3 SC_Clock_out+	21	22	V3 SC_Clock_out-
	V1 FRAME IN	23	24	V1 FRAME OUT
	V3 FRAME IN	25	26	V3 FRAME OUT
	GND	27	28	GND
	V3 BUSY	29	30	V3 PROG
	V3 INIT	31	32	V3 DONE
	V3 CS_B	33	34	V3 ECHO DONE
	V3 CCLK	35	36	V3 D0
	GND	37	38	GND
	POWER OFF OUTPUT	39	40	*LVCMOS25 SPARE*
	LVCMOS25 SPARE	41	42	*LVCMOS25 SPARE*
	LVCMOS25 SPARE	43	44	*LVCMOS25 SPARE*
	LVCMOS25 SPARE	45	46	*LVCMOS25 SPARE*
	GND	47	48	GND
To Front of Module	SPARE 5 (LVDS/LVCMOS)	49	50	SPARE 6 (LVDS/LVCMOS)

SEGMENT POWER to CONTROL card connector A connections

	Connector A			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	V4 SC_Clock_in+	1	2	V4 SC_Clock_in-
	V4 SC_Data_in+	3	4	V4 SC_Data_in-
	V4 SC_Data_out+	5	6	V4 SC_Data_out-
	V4 SC_Clock_out+	7	8	V4 SC_Clock_out-
	V3 SC_Clock_in+	9	10	V3 SC_Clock_in-
	V3 SC_Data_in+	11	12	V3 SC_Data_in-
	V3 SC_Data_out+	13	14	V3 SC_Data_out-
	V3 SC_Clock_out+	15	16	V3 SC_Clock_out-
	SPARE 1 (LVDS/LVCMOS)	17	18	SPARE 2 (LVDS/LVCMOS)
	SPARE 3 (LVDS/LVCMOS)	19	20	SPARE 4 (LVDS/LVCMOS)
	GND	21	22	GND
	V1 TEMP EN 0	23	24	V1 TEMP EN 1
	V2 TEMP EN 0	25	26	V2 TEMP EN 1
	V3 TEMP EN 0	27	28	V3 TEMP EN 1
	V4 TEMP EN 0	29	30	V4 TEMP EN 1
	P/S TEMP EN 0	31	32	P/S TEMP EN 1
	TEMP DATA	33	34	TEMP CLK
	GND	35	36	GND
	COMMS RESET	37	38	VIRTEX CLOCK ENABLE
	VCC IO 3.3Volts	39	40	VCC IO 3.3Volts
	VCC IO 3.3Volts	41	42	VCC IO 3.3Volts
	VCC IO 2.5Volts	43	44	VCC IO 2.5Volts
	VCC IO 2.5Volts	45	46	VCC IO 2.5Volts
	GND	47	48	GND
To Front of Module	NOT CONNECTED	49	50	VCCINT 1.8V MONITOR

SEGMENT POWER to CONTROL card connector B connections

	Connector B			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	V1 SC_Clock_in+	1	2	V1 SC_Clock_in-
	V1 SC_Data_in+	3	4	V1 SC_Data_in-
	V1 SC_Data_out+	5	6	V1 SC_Data_out-
	V1 SC_Clock_out+	7	8	V1 SC_Clock_out-
	V1 SC FRAME IN	9	10	V1 SC FRAME OUT
	GND	11	12	GND
	V3 BUSY	13	14	V3 PROG
	V3 INIT	15	16	V3 DONE
	V3 CS_B	17	18	V3 ECHO DONE
	V3 CCLK	19	20	V3 D0
	GND	21	22	GND
	V4 BUSY	23	24	V4 PROG
	V4 INIT	25	26	V4 DONE
	V4 CS_B	27	28	V4 ECHO DONE
	V4 CCLK	29	30	V4 D0
	GND	31	32	GND
	MODE 0	33	34	MODE 1
	MODE 2	35	36	RDWR_B
	GND	37	38	GND
	D1	39	40	D2
	D3	41	42	D4
	D5	43	44	D6
	D7	45	46	GND
	GND	47	48	GND
To Front of Module	GND	49	50	GENERAL RESET

SEGMENT POWER to CONTROL card connector C connections

	Connector C			
	Signal name	**Pin**	**Pin**	**Signal name**
To Rear of Module	SEG/CORE SC_Clock_in+	1	2	SEG/CORE SC_Clock_in-
	SEG/CORE SC_Data_in+	3	4	SEG/CORE SC_Data_in-
	SEG/CORE SC_Clock_out+	5	6	SEG/CORE SC_Clock_out-
	SEG/CORE SC_Data_out+	7	8	SEG/CORE SC_Data_out-
	SEG/CORE FRAME IN	9	10	SEG/CORE FRAME OUT
	GND	11	12	SEGMENT POWER OK IN
	V2 FRAME IN	13	14	V2 FRAME OUT
	V2 SC_Clock_in+	15	16	V2 SC_Clock_in-
	V2 SC_Data_in+	17	18	V2 SC_Data_in-
	V2 SC_Data_out+	19	20	V2 SC_Data_out-
	V2 SC_Clock_out+	21	22	V2 SC_Clock_out-
	V4 FRAME IN	23	24	V4 FRAME OUT
	V3 FRAME IN	25	26	V3 FRAME OUT
	GND	27	28	GND
	V1 BUSY	29	30	V1 PROG
	V1 INIT	31	32	V1 DONE
	V1 CS_B	33	34	V1 ECHO DONE
	V1 CCLK	35	36	V1 D0
	GND	37	38	GND
	V2 BUSY	39	40	V2 PROG
	V2 INIT	41	42	V2 DONE
	V2 CS_B	43	44	V2 ECHO DONE
	V2 CCLK	45	46	V2 D0
	GND	47	48	GND
To Front of Module	SPARE 5 (LVDS/LVCMOS)	49	50	SPARE 6 (LVDS/LVCMOS)