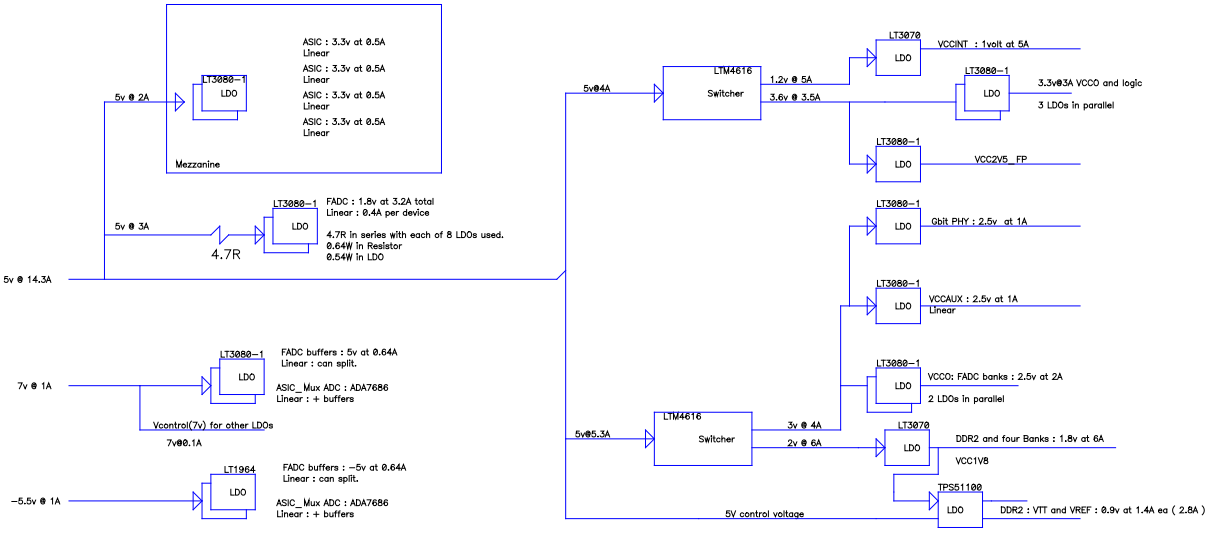
FEE64 power supply system Revision A

The Revision A of the power supply system is designed to remove as many switching convertors as possible. All supplies are now sourced through linear regulators and the switching regulators are reduced from 11 to 4. (two dual modules). The voltage these switchers operate from is reduced from +30v to +5v. This reduces the likely EMI effect of the switching.



Mezzanine supply changes from 4v to 5v and is connected directly to the external +5v linear power supply.

FADC AD9252 supplies are currently sourced using a 2.5v intermediate voltage. There is one low voltage dropout regulator, LDO, per FADC. These will now be connected directly to the external +5v linear power supply. The increase in voltage drop will cause an increase in temperature in the LDO. The power loss is (5v-1.8v)*0.37 => 1.18W. This is mitigated by a resistor in series with each LDO which will dissipate 0.64W leaving the LDO with 0.54W. The LDO has a junction temperature +60 degrees per watt above ambient. With the DOW Corning foam and water cooling the junction should be at 91 degrees. The maximum for the junction is 125 degrees. The LDO has over temperature protection.

FADC buffer positive supplies are currently sourced from a 5.5v intermediate voltage. There is one LDO (LT3080) per 8 dual buffer devices. These will now be connected directly to the external +7v linear power supply. The buffers have been changed to reduce the bandwidth and current consumption. Each LDO will dissipate 0.32W.

FADC negative supplies are now direct from an external supply. The changes will be to use a negative LDO per 8 dual buffer devices. These will be connected directly to the external -6v linear power supply.

The Logic supplies for the FPGA and peripherals are sourced from 5v powered DC-DC convertors. There are four voltages from two dual output 8A modules. The switchers are required to make the power losses and associated junction temperatures in the LDOs fall within reasonable ranges.

Module 1: ch1 => 1.2v. This is regulated for VCCINT (1v) using an LT3070 5A regulator designed to be used for this purpose.

Module 1:ch2 => 3.6v. This is regulated to give four supplies.

VCCO3V3 using three LT3080 1A LDOs. These can be paralleled to share the current load.

VCC2V5_FP for the interfaces to the BuTiS clock box interfaces using a single LT3080 1A LDO.

Module 2:ch1 => 2v. This is regulated for VCC1V8 (1.8v) using an LT3070 5A regulator designed to be used for this purpose.

VTT and VREF are generated for the DDR2 SDRAM from the VCC1V8 using a TPS51100 linear regulator designed for this purpose. This device requires a +5v logic supply which will be derived directly from the external +5v linear power supply via a filtering network.

Module 2:ch2 => 3v. This is regulated to give three supplies.

VCCO2V5 using two LT3080 1A LDOs. These can be paralleled to share the current load.

VCCAUX (2.5v) using a single LT3080 1A LDO.

VCC2V5_GBIT (2.5v) for the Gbit Ethernet PHY using a single LT3080 1A LDO.

The LT3080 LDOs require a control voltage that is 1.2v higher that the output voltage. This ranges from +7v to +4v. The intention is to source this from a separate +7v supply.

The external power supply must now source +5v at 15amps, -6v at 1amp and +7v at 1amp.

LTM4616 design decisions

SVIN – internally connected to Vin
SGND – connect to GND with layout guidelines.
MODE – tie to GND for continuous mode.
CLKIN – Leave floating.
PLLLPF – leave floating.
PHMODE – leave floating
MGN – connection depends on output voltage.
BSEL – leave floating. Margining not required.
Track – connect to SVin to disable tracking.
FB – Resistor to GND to program the output voltage.
ITHM – Connect to SGND.
PGOOD – Open drain indication output is +/- 10% from programmed.
RUN – Voltage above 1.5v turns on the convertor.
SW – test point.
CLKOUT – Used for multiple module operation. Not required in this design.

Resistor values for design voltages.

1.4v@5A : Rfb = 7.41k
3.6v@6A : Rfb = 1.98k
2.2v@6A : Rfb = 3.70k
3v@5A : Rfb = 2.46k

Power loss is dependent on current. 3.5A => 0.9W, 4A => 1W, 5A => 1.2W, 6A => 1.5W. The supplies are split between two modules to give 2.5W and 2.1W. Junction temperature needs to be kept above 115C otherwise the module restricts the current. Theta Ja is about 10C/W.

Input capacitors. The need is for a bulk capacitor of 100uF. There are 3 x 10uF capacitors in the module. Part is TDK C4532X5ROJ107MZ or Murata GRM32ER60J107M.

Output capacitors. The same is used at all four outputs. 470uF : SANYO poscap : 4TPE470M. 1 x 22uF: TDK C3216X7S0J226M or Murata GRM31CR61C226KE15L.

Linear regulator design notes.

LT3080: Added a 10/22pF capacitor across the Rset. Added a 1.5K resistor to GND at the output of those providing 1.8v to the FADCs as they need a minimum load of 1mA to regulate and the FADCs can be powered down.
To operate in parallel for increased current the Rset = Vout/10uA x N. Where N is the number of LT3080s used. Only one Rset is used for all devices and the Set inputs are commoned.

LT3070:

Listing of all the power distribution and where it goes.

Power supply name	Power source	Routing Layer(s)	Complete ?
Pwrin+5v	External	AN_Pwr	
Pwrin+7v	External	Power & Sig3	
Pwrin-6v	External	Bottom, Power & Sig2	
Vccint_inter_1v4	Pwrin+5v	Top & Bottom	
Vcc3v3_inter_3v6	Pwrin+5v	Bottom	
Vcc1v8_inter_2v2	Pwrin+5v	Top & Bottom	
Vcc2v5_inter_3v0	Pwrin+5v	Sig1	
Buff-5v_A	Pwrin-6v	Bottom	✓
Buff-5v_B	Pwrin-6v	Bottom	✓
Buff-5v_C	Pwrin-6v	Bottom	✓
Buff-5v_D	Pwrin-6v	Bottom	✓
Buff+5v_A	Pwrin+7v	AN_Pwr	✓
Buff+5v_B	Pwrin+7v	AN_Pwr	✓
Buff+5v_C	Pwrin+7v	AN_Pwr	✓
Buff+5v_D	Pwrin+7v	AN_Pwr	✓
Vcontrol	Pwrin+7v		
VCC_5V_RDO	Pwrin+7v	AN_Pwr	✓
VCC3V3_RDO	Pwrin+7v	Sig1	✓
VCC2V5_RDO	Pwrin+7v	Sig3	✓
VCC_-5v_RDO	Pwrin-6v	Power	✓
VREF_DDR	DDR2_VCC1V8 & Pwrin+5v	Sig4	✓
DDR2_Control_VTT	DDR2_VCC1V8	Bottom	✓
DDR2_VCC1V8	Vcc1v8_inter_2v2	Top and Power	✓
VCC_FADC1V8_A	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_B	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_C	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_D	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_E	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_F	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_G	Pwrin+5v	AN_Pwr	✓
VCC_FADC1V8_H	Pwrin+5v	AN_Pwr	✓

VCC_FADC_DRVDD	Pwrin+5v	Sig1 & Sig2	✓
VCCO2V5	Vcc2v5_inter_3v0	Power	✓
VCCAUX	Vcc2v5_inter_3v0	AN_Pwr	✓
VCCINT	Vccint_inter_1v4	AN_Pwr	
VCC3V3	Vcc3v3_inter_3v6	Power	
VCC2v5_GBIT	Vcc2v5_inter_3v0	Power	
PHY_AVDD0	VCC2v5_GBIT	Power	✓
VCC2v5_FP	Vcc3v3_inter_3v6		
SYSMON_AVDD	Pwrin+7v		