Exogam Project

GIR_BGA MAP

for

GOCCE

Ver 1.1

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1 GOCCE DESCRIPTION:

1.1 GOCCE in Exogam:

The EXOGAM segmented clover is composed of 4 high purity Ge crystals, 4 segments surround each crystal, which gives a total of 16 segments per clover. The segments collect the positive charge of a gamma ray, which is the same charge collected on the central contact. The energy is divided randomly on the 4 segments depending on the position and the angle of the gamma ray impact. An energy measurement on the 4 segments of the same crystal is needed every time a gamma ray hits it and the inner contact Constant Fraction Discriminator (CFD) triggers. Also timing measurements between the discriminator of each adjacent hit segment and a software selectable signal must be measured. This signal could be the inner contact CFD, the Fast Trigger, the Exogam beam pulse, or any needed signal. The outer contact card (GOCCE) uses the associated veto from the ESS (Exogam Escape Suppression Shield) card for Compton suppression. The inner contact CFD is the start signal for GOCCE. Therefore GOCCE is a slave card.

1.2 GIRV5 in GOCCE.

The *GIRV5* is a Readout Interface card, which is connected between the *VXI* back plane and the GOCCE *Analogue* card, so that the 2 cards (*GIRV5-Analog*) form a complete *VXI* D-size Board. This Board have programmable Input/ Output signals and assumes the analogue part configuration, the Readout interface logic (internal, and external), the *VXI* power supply filtering, the Inspection lines control logic, the *DSP* control for online data processing as well as data acquisition parameters for *EXOGAM*. Connections between GIRV5 and GOCCE card is done by 3 AP connectors with 150 pins each.

The *GIRV5* 's job is to read out the corrected *ADC* data and writes them (or not) into the *FIFO's*, then these data are transferred to the *VRE* (VXI Readout Engine) Board on the *VXI* back plane. The Readout mechanism is completely programmable, and suitable for any acquisition system. In the case of *EXOGAM, Eurogam* Readout interface for common deadtime is used.

1.2.1 DSP online data processing:

1.2.1.1 Multiprocessing Control:

This new feature is added to interconnect any assembly of *VXI* cards *DSP's* together through the *VXI* Local bus. This feature is completely programmable. That is by software control we can specify graphically which *VXI* cards can be grouped together through the Local bus, so that the *DSP* can have data exchange for Readout decision, and in this way we can decide in a more accurate way if the data in the *FIFOs* are good data or not. In another context, this decision acts as a trigger level which could be called *Readout trigger*, that is after the data are sent to the *FIFO's* the *DSP* can make some analysis on these data, and can interrupt the external Readout cycle if those analysis don't correspond to what the user needs.

1.2.1.2 Power Supplies Control and automatic Pole Zero Adjustment.

Other feature for the *DSP* is Local control on the *VXI* card for Analogue signal through a 16 input Analogue multiplexer; there are 2 free Analogue flags on the AP connector, the Analogue Inspection Lines as well as the Voltage inspection line are connected to this multiplexer, and the VXI power supplies are connected too. We can, for example, control the power supplies and send flags when their level go up the references.
We can also control the Automatic Pole Zero Adjustment specific for *Ge* detectors or other detectors which need Pole Zero Adjustment[1] or other Automatic Dac Adjustment (by *DSP* Programming). This multiplexer is connected to a local high Speed 66MHz Flash *ADC*, then the values are written in the *DSP RAM*, after which the *DSP* Processes the data, and send the correction to the *Software on-line* control through flag registers.

1.2.1.3 On-Line Histogrammer and Datas Processing.

DSP process ADC data and builts spectra in its external memory (Spy mode). DSP can also process datas (gain adjustment) before sending them to FIFO (Filter mode). The external memory can store 128 spectra of 14 bits (1M words of 32 bits).

Spy mode: In this mode the *DSP* just collects the data at the same time, as they go onto the *VXI* backplane, during an event and make processing on these data, and puts the result in its Memory. This can help the user to check on the results inside each card during an experiment to make sure that the card setup is done good. The *DSP* DOES NOT make any modification on the good data .

Filter mode: The *GIRV5* can be programmed by software to make the *DSP* read the data without sending it to the *VXI* backplane, and then the *DSP*, automatically, makes data processing, and sends back the results to *GIRV5* readout interface which sends it back to the *VXI* backplane. In this mode the *DSP* can make any kind of filtering on the data, and even keeps the raw results, and add more processed data inside the same event. This method can help the user to get more information from each event in addition to the raw data.

1.2.2 Readout Mechanism:

The Readout Mechanism will be divided into two cycles: Internal, and External Readout cycles. The Internal cycle is the cycle which takes place for data transfer between the *Analogue* card, and the *GIRV5*. While the External Readout cycle is the interface between the *G.I.R*, and the *VRE* Board.

The GOCCE is a slave card, but it can be used as a Master card for tests. The start signal for the event processing is the inner contact delayed CFD. When the CFD triggers, the corresponding channel will open the 4 PDS gates of the 4 corresponding segments. The channel Local Trigger will start 3 timers to look for Fast Trigger and Validation or the Watchdog Timeout if it was an error or noise that starts the channel acquisition. All events are synchronised with the EXOGAM Trigger. The CFD is delayed by 2 µs to look for segment DTD signals to measure segment timing, each segment DTD will start a TDC counter, and the delayed CFD will Stop all the 4 TDCs. At the end of the PDS gate (and assuming that the event is a good event) a convert signal is sent to the 4 ADCs simultaneously. When the ADC busy line is de-asserted, the

[1] Not for GOCCE

readout FPGA sends 16 clock pulses to readout the ADCs; this means that the serial clocks will not disturb the ADCs during coding which is very important to noise reduction. At the end of ADC readout, which is the maximum time to wait for validation, a start readout will be sent to the GIR, and an internal readout cycle will write both the ADC, and TDC (if available) data into the FIFO. Then a classical VRE to VXI back-plane block data readout transfer cycle starts to readout all non empty FIFO (see timing diagram below).

The GOCCE will be possible to run (triggering and analysis of the analogue treatment) in crystal mode or in clover mode.

Crystal mode:

In Crystal mode each clover detector crystal is considered as one detector. Each crystal acquisition is processed individually. In another way the GOCCE channel will start acquisition from its corresponding inner contact CFD, and it will receive the veto from the corresponding suppression shield. Also the triggering and subsequent analysis of the 4 OUTER segments are managed by the INNER CFDs and VETOs of the associated crystal only.

Clover mode:

In Clover mode (i.e. 4 crystals) triggering and analogue treatment is made in common for the 16 OUTER contacts by the OR of the 4 Inner CFD and VETO signals of the clover detector.

1.2.3 Electrical and Mechanical precautions:

This card is specifically designed for low noise Analogue data acquisition systems. It takes care of the *EMC* problems. It already contains several elements which worked before in other similar cards. Data transfer is 20 Mbytes/sec 5 Mwords/sec, and in *Nuclear* physics data acquisition systems the shaping time and the coding time take highest percentage of the total channel dead time.

The aim of this Board is to have Readout interface completely programmable for different Readout mechanisms, and which can be suitable for different data acquisitions. That is it can be adapted to either fast or slow data transfers. The Analogue engineer need not be anxious about the Readout part of his Board. He needs only to design his Board up to digital data, and then he has to choose the Readout system to be adapted for his experiment, so that the Readout interface can be built.

EMC problems are very dangerous to sensitive Analogue signals, especially in *Nuclear* physics data acquisitions. *GIRV5* has the middle column of the 150 pin *AP* connectors (as shown previously) mostly grounded. Extra flat connectors will be used to minimise the electromagnetic noise penetrations. Slow asynchronous data transfer from the *FIFO's*. (see the *PCB_AP* connections diagram.). For example the 2 *Analogue* Inspection Lines are surrounded with ground pins. Power Supply chokes, and *OSCON* capacitors are used to filter the *VXI* power supplies.

The interconnection between the *Analogue* card and *GIRV5* can be shown in the figures below showing the top, bottom, and face views. An extractor tool is built to extract the *PCB_AP* connector (450 pins) out of both the *GIRV5*, and the *Analogue* card.

A new mechanic has been adopted to protect cards from high temperature and EM perturbations. The card is now fixed on 2 rails (upper and lower) and the whole is inserted in the crate slot. This has induced the decrease of the PCB dimensions, but the manipulation of the card during prototype tests is easier and safer. The rails are pierced with 450 holes each, increasing the airflow area about 50%. 2

shields are fixed by 36 screws in the rails, avoiding the alignment problem causing by the passage through the PCB in the old mechanic. EMC performances are above 90dB.

1.3 GOCCE Specification:

1.3.1 Input / Output Signals on the front Panel:

- Input Signals.
  - 20 Inputs: 16 inputs are used for the clover preamplifiers, and 4 spares. The spare inputs, are located as 1 input per clover crystal.
  - 4 Inner CFD signals from the HRGe8x card.
  - 4 Veto signals from the ESS card.
- Output Signals.
  - 4 Inner CFD output signals to the ESS card (TBD1).
  - 4 Veto outputs to the HRGe8x card (TBD).

1.3.2 Motherboard Description

- Analogue functions per segment:
  - Shaping Amp with ranges from 30 keV to 6 MeV with an intrinsic resolution of 0.3 keV. The peaking time is 7 µs which corresponds to a 3 µs time constant.
  - Timing Filter Amplifier (TFA) associated to a Double Threshold Discriminator (DTD). Threshold from 30 to 700 keV with 3 keV resolution (256 steps).
  - Peak Detector and Stretcher (PDS) associated to a 14 bit ADC with a DNL of +-5%, to have 3 keV resolution. There are 5 PDS-ADC inputs per daughter board.
- Logic per segment included inside re-programmable FPGA (SALTI 16):
  - 12 bits TDC (started by individual DTD and stopped by the corresponding 2 µs delayed inner CFD) with a resolution of +/-10 ns.
  - 32 bit scalers for the DTD counting rate measurements.
  - 4 qualifiers bits (pre-pileup, post pileup, Veto, pre-or-post-pileup).
    - ✓ 2 qualifiers with the ADC word (veto, and pre or post-pileup).
    - ✓ 2 Qualifiers with the TDC word (pre-pileup, and post-pileup).
  - Low Threshold window : This register filters the low data values to be read out.
- Logic per channel (4 segments):
  - Complete digital Local Trigger to check for event synchronisation between the inner CFD and the Master Trigger. It contains 3 counters (2 for the sample point detection, and one timeout register), and pileup Logic
- Other control logic.
  - Generates a digital controlled PDS gate delay wrt (with respect to) inner CFD.
  - Controls all ADC logic, convert, readout, and sliding scale update, and correction.
  - Generates acknowledge for a good event to be read out.
  - Internal Readout interface with the GIR DSP, and FIFO.
  - A common stop (from inner CFD delayed by 2 µsec) for the four TDCs of the four adjacent segments.
  - A veto logic from the ESS card to mark or reject compton suppression events.
  - VME interface to load ADC group and item registers, sample point adjustments, delays, timeout registers, test mode configurations and internal digital inspection lines.

[1] Tbd: To be discussed

L.A.& TFA
DTD
ADC & PDS
5 SEGMENTS
SPACE
Segments
Pulse
Analysis
Card for
Exogam
G.I.R. V5

1.4 GOCCE AP Connector Description:

1.4.1 General description.

AP1:

- 76 Input/ Output pins (called Reg_Io) which are fully programmable pins of a *XILINX FPGA*
- 10 bits of a latched address bus (*ADD* 1 to *ADD* 10).
- Filtered -2 volts *VXI* power supply.
- 1 *Analogue Flag* free signal which is connected to an analogue multiplexer inside the GIRV5, and which can be digitised by the DSP program.
- 3 LEDs : Temperature, Fifo error, Done GIR LCAs.

AP2:

- The higher 16 bit of a latched address bus (ADD 11 to ADD 23).
- Analogue, Digital, and Voltage[1] Inspection Lines which come from the Analogue card.
- the lower 16 bits of the bi-directional data bus.
- 16 input/output reprogrammable pins (called Reg_Io) from XILINX FPGA (LCA Decode2).
- 18 input/output pins from the BGA LCA (READ 0 to READ 17 except READ 6,8,10,11,14 which are buffered output signals to the Analogue card.
- 4 TTL signals which come from the VXI back plane as ECL signals (they are the Trigger Event numbers in EXOGAM)
- TEMP flags : Under et Over flags for sensor 1 and 2.

AP3:

- The higher 16 bits of the data bus (DATA 16 to DATA 31).
- 5 input/output signals from the BGA LCA (READ 18 to READ 22).
- The Differential VXI line Starx +/- , and 2 TTL Trigger lines (which is the Fast Trigger, Validation, and Inhibit signals respectively). They are the EXOGAM MASTER Trigger signals.
- Moreover there are 49 INPUT/output pins from LCA Decode2 (called Reg_IO).
- 4 bits which are connected to the highest nibble in the FIFO, they are the event no. latched in the Analogue Board.
- 3 TTL signals which can be used as flags for the DSP.
- 1 *Analogue Flag* free signal which is connected to an analogue multiplexer inside the GIRV5, and which can be digitised by the DSP program.
- The VME 16 MHz Clock, and filtered +/- 12 volts VXI power supply.

[1] voltage line is not connected for GOCCE

1.4.2 Detailled description.

1.4.2.1 AP1 :

- **DAC signals (7 or 8):**
  - **DDIN, DCLK, DReset[1]:** Serial data, Clock, and Reset signals common for all chips
  - **DCS A, B, C, D, Spare :** one chip select signal per channel plus one for spare segments.
- **CCR signals (7) :**
  - **CCRDIN, CCRCLK, CCR_Rst :** Serial Data, Clock and Reset signals for active segments.
  - **SCCRDIN, SCCRCLK, SCCR_Rst :** Serial Data, Clock and Reset signals for spares segments.
- **GO*/Stop :** Go and Stop acquisition.
- **Mux signals (10) :**
  - **ClkMux A, B, C, D, Spare :** one clock signal per channel plus one for spare segments.
  - **DataMux A, B, C, D, Spare :** one data signal per channel plus one for spare segments.
- **Temperature signals (5) :**
  - **CLKTemp, DataTmp :** Clock and data signals common for the 3 sensors.
  - **RstTmpDtd, RstTmpSp, Rst_R_In :** one Reset signal per sensor. (DTD, Air_in, spare)
- **ADD[10:2] :** this is the lowest byte of the *VME* Address bus, it is enabled by the *GIRV5*
- **43 Reg I/O 1 available.**
- **Temp Led** : ON if Over or under normal temperature.
- **Error Led** : ON if Fifo Error.
- **Done Led :** ON if all LCAs are programmed.
- **VPTAT 1 :** Temperature Monitoring Sensor 1.
- **+5 V :** 6 pins. **-5.2 V :** 6 pins. **-2 V :** 8 pins.

1.4.2.2 AP2 :

- **Clk GIR : 33MHz or 40 MHz.**
- **Last Pass :** Renout of the analogue card indicates end of readout cycle.
- **StartRdt :** This signal is the Start_Readout of the analogue card, which is the back edge of the last *Busy* signal.
- **Valack :** this signal is the *Validation Acknowledge* for VXI Readout cycle.
- **Dtready :** Signal given by analogue card when a data is ready to go to the FIFO.
- **Renin :** Start readout cycle of events, this signal is sent by GIR to the analogue card.
- **AI** 1,2 **:** Analogue Inspection Lines 1 and 2.
- **DI** 1,2 **:** Digital Inspection Lines 1 and 2.
- **ADD[23:11] :** *VME* Address bus, it is enabled by the *GIR*
- **DATA[15:0] :** these bits are the 16 LSB *GIR* Data bus.
- **EvtIn [3:0] :** 4 bits Event Number from Lbus.
- **EvtAna [3:0] :** 4 bits Event Number to GIR Readout
- **LTResetGir :** This signal indicates the end of the event processing. It goes to *the analogue card* which sends it to the *Local Triggers* that were read out.
- **Dtack :** buffered data acknowledge signal for each word of the *the analogue card* in readout cycle.
- **Global Reset :** buffered global reset signal.
- **OVER 1,2 *, UNDER 1,2 *:** Indicates over temperature for sensors 1 and 2
- **Spare_Readout[5:0]** : Spare connexions between LCA_BGA GIR and GOCCE.

[1] To be discussed

– **+5 V : 6 pins. -5.2 V :** 6 pins. **+12 V :** 4 pins. **- 12 V :** 4 pins.

1.4.2.3 AP3 :

– **39 Reg I/O 2 available.**
– **DATA[31..16] :** these bits are the 16 MSB *GIR* Data bus.
– **R/W :** buffered *VME* read-write signal.
– **DtAck_VME :** buffered data acknowledge signal for each word of the GOCCE read by the VXI external readout.
– **OE_Data_AP :** Driven each time the analogue part is adressed.
– **DIR_Data_AP :**
– **Inhibit* :** buffered *Inhibit* signal from the *MASTER Trigger*
– **Fast Trigger :** buffered *Fast Trigger* signal from the *MASTER Trigger*.
– **Val* :** buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).
– **Beam RF :** Beam signal
– **Linkbus2 :** link port between DSP GIR and GOCCE.
– **PromCS , RD, WR, hd :** serial PROM control signals of the *GOCCE* card.
– **CLK16MHz**
– **FTECL+/- :** Fast Trigger signal in ECL mode.
– **WR_Strobe :** Latch data between GOCCE and GIRV5.
– **CS_GOCCE** : signal to select the GOCCE memory range.
– **Clk100MHz :** Clock 100 MHz frequency in ECL mode.
– **VPTAT 2 :** Temperature Monitoting Sensor 2.
– **DSPFLAG 1to 3 :** TTL signals which can be used as flags for the GIR DSP
– **+5 V : 6 pins.-5.2 V :** 6 pins. **+24 V :** 4 pins. **-24 V :** 4 pins.

1.4.3 Pinouts of the AP Connector for the GOCCE Card

	AP1 Connector			AP2 Connector			AP3 Connector			
	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	
1	+5 V	+5v	+5v	+5 V	+5 V	+5 V	+5v	+5v	+5v	1
2	DDIN	GND	DCLK	ClkGIR	GND	ADD 11	DATA 16	GND	*IO_B38*	2
3	DCSA	Temp LED	DCSB	LastPass	LedDspGir	ADD12	DATA 17	DSPFLAG	*IO_B40*	3
4	DCSC	GND	DCSD	StartRdt	GND	ADD13	DATA 18	GND	*IO_B42*	4
5	DCS_Spare	error LED	Dac_Rst	Valack	Under 1	ADD14	DATA 19	DSPFLAG	*IO_B38*	5
6	CCRDIN	GND	CCRCLK	SpareRdt0	GND	ADD15	DATA 20	GND	*IO_B40*	6
7	CCR_Strb	DONE	CCR_RST	DtReady	Over 2	ADD16	DATA 21	DSPFLAG	*IO_B42*	7
8	SCCRDIN	GND	SCCRCLK	Renin	GND	ADD17	DATA 22	GND	*IO_B38*	8
9	SCCR_Strb	VPTAT1	GO*/STO	GND	Under 2	ADD18	DATA 23	VPTAT2	*IO_B40*	9
10	ClkMuxA	GND	DataMux	AI 1	GND	ADD 19	DATA 24	GND	*IO_B42*	10
11	ClkMuxB	GND	DataMuxB	GND	GND	ADD 20	DATA 25	GND	*IO_B38*	11
12	ClkMuxC	GND	DataMuxC	AI 2	GND	ADD 21	DATA 26	GND	*IO_B40*	12
13	ClkMuxD	GND	DataMux	GND	GND	ADD22	DATA 27	GND	GND	13
14	SClkMux	GND	SDataMux	DI 1	GND	ADD23	DATA 28	GND	FTECL+	14
15	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	15
16	CLKTEM	GND	DataTmp	DI 2	GND	GND	DATA 29	GND	FTECL-	16
17	RstTmpDt	GND	RstTmpSp	GND	GND	GND	DATA 30	GND	*IO_B11*	17
18	RST_R_IN	GND	RegI/O 1	VI	GND	GND	DATA 31	GND	*IO_B12*	18
19	RegI/O 1	GND	RegI/O 1	DATA 0	GND	NC	*IO_B13*	GND	**WrStrobe**	19
20	RegI/O 1	GND	RegI/O 1	DATA 1	GND	GND	*IO_B14*	GND	**CSGocce**	20
21	RegI/O 1	GND	RegI/O 1	DATA 2	GND	EvtIn0	**R/W**	GND	NC	21
22	RegI/O 1	GND	RegI/O 1	DATA 3	GND	EvtIn1	**DtAckVme**	GND	*IO_B15*	22
23	RegI/O 1	GND	RegI/O 1	DATA 4	GND	EvtIn2	**OEDataAP**	GND	*IO_B16*	23
24	RegI/O 1	GND	RegI/O 1	DATA 5	GND	EvtIn3	**DirDataAp**	GND	*IO_B17*	24
25	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	25
26	RegI/O 1	GND	RegI/O 1	DATA 6	GND	EvtAna0	**Inhibit***	GND	*IO_B18*	26
27	RegI/O 1	GND	RegI/O 1	DATA 7	GND	EvtAna1	**FT**	GND	*IO_B19*	27
28	RegI/O 1	GND	RegI/O 1	SpareRdt1	GND	EvtAna2	**Val***	GND	*IO_B20*	28
29	RegI/O 1	GND	RegI/O 1	DATA 8	GND	EvtAna3	**BeamRF**	GND	*IO_B21*	29
30	RegI/O 1	GND	RegI/O 1	DATA 9	GND	GND	Link2D0	GND	*IO_B22*	30
31	RegI/O 1	GND	RegI/O 1	DATA 10	GND	GND	Link2D1	GND	*IO_B23*	31
32	RegI/O 1	GND	RegI/O 1	DATA 11	GND	GND	Link2D2	GND	*IO_B24*	32
33	RegI/O 1	GND	RegI/O 1	DATA 12	GND	GND	Link2D3	GND	*IO_B25*	33
34	RegI/O 1	GND	RegI/O 1	DATA 13	GND	RegI/O 2	Link2Clk	GND	*IO_B26*	34
35	RegI/O 1	GND	RegI/O 1	DATA 14	GND	RegI/O 2	Link2Ack	GND	*IO_B27*	35
36	RegI/O 1	GND	RegI/O 1	DATA 15	GND	RegI/O 2	*PromCS*	GND	*IO_B29*	36
37	ADD2	GND	RegI/O 1	SpareRdt2	GND	RegI/O 2	*PromRd*	GND	*IO_B31*	37
38	ADD3	GND	RegI/O 1	Inh_Req	GND	RegI/O 2	*PromWr*	GND	*IO_B33*	38
39	ADD4	GND	RegI/O 1	**LTResetGir**	GND	RegI/O 2	*PromClk*	GND	*IO_B35*	39
40	ADD5	GND	RegI/O 1	**Dtack**	GND	RegI/O 2	*Promhd*	GND	*IO_B37*	40
41	ADD6	GND	RegI/O 1	SpareRdt3	GND	RegI/O 2	*IO_B38*	GND	*IO_B39*	41
42	ADD7	GND	RegI/O 1	SpareRdt4	GND	RegI/O 2	*IO_B40*	GND	*IO_B41*	42
43	ADD 8	GND	RegI/O 1	**SpareRdt5**	GND	NC	*IO_B42*	GND	*IO_B43*	43
44	ADD 9	GND	RegI/O 1	**EMCR3**	GND	NC	**Clk16M**	GND	Clk100M+	44
45	ADD 10	GND	Memech*	**GlobReset**	GND	NC	*IO_B44*	GND	Clk100M-	45
46	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	46
47	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	47
48	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	48
49	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	49
50	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	50

LCA 1 LCA 2 Not Connected **Buffered Outputs** Fixed signals

2 GOCCE MEMORY MAP:

VME Address	*Function*
0xFFFFFF80 to 0xFFFFFF8A	VXI Configuration Registers. *(See § 2.1)*
0x0 to 0xFFFFFC	GIR and Analog card Area Address *(See §2.2)*
0x1000000 to 0x2FFFFC	SPACE Area Address*(See § 2.3)*

2.1 VXI Configuration Registers.

VME area address : 0xFFFFFF80 to 0xFFFFFF8A

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

VXI Base Address (slot 1)	*Description*	*DATA Format*
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8A	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

Procedure to write in GIR Prom ID :

- Put the strap on S1 (card TOP side)
- Wrw rmShortaddress(slot)+0x4,0x8 ➔ write mode
- Wrw rmShortaddress(slot)+0x0,0x5A.➔ IN2P3 code
- Wrw rmShortaddress(slot)+0x2,0x10➔ Card Type (0xC10 for GOCCE)
- Wrw rmShortaddress(slot)+0x8,0x1 ➔ GIR number (0x1 to 0x14)
- Wrw rmShortaddress(slot)+0xA,0x???? ➔ Card level number (0x52 for GOCCE card)

Cfglist display : DF00, 6C10, F95C, 0400, DF00, DF52

Enable Clk16MHz on ap connector :

- Wrw rmShortaddress(slot)+0x4,0xFFF3 ➔ bit2 = 0, enable Clk16MHz

2.2 GIR and Analogue Area.

VME area address : (0x000000 to 0xFFFFFC):

VME Memory Addresses	Function
0x000000 to 0x7FC	GIR Area Address *(See § 2.2.1)*
0x000800 to 0xFFC	Analog Card (SALTI Area) Common Area *(See §2.2.2)*
0x1000 to 0x4FFC	Channel (SALTI Area) Area Address (See § 2.2.2)
0x200000 to 0x3FFFFC	GIR External Memory Area Address (See § 2.2.3)
0x400000 to 0x4BFFFC	GIR DSP Area Address (See § 2.2.4)

2.2.1 GIR Register Area

VME area Address : 0x000000 to 0xFFC

VME Address	Bus Width	Rd/ Wr	Function
0x0 to 0xE	16	w	*Not yet allocated*
0x10	16	w	GIR Module Control Register (GMCR) *(See § 2.2.1.1)*
0x12	16	rw	Analog card Module Control Register (AMCR)
0x14	16	w	DSP DAC Adjustment
0x16	16	w	DSP Pot Adjustment
0x18 to 0x1E	16	w	*Not yet allocated*
0x34 to 0x3E	16	w	*Not yet allocated*
0x40--0x5E	16	r/w	Temperature control Register *(See §2.2.1.2)*
0x60 to 0xFE	16	w	*Not yet allocated*
0x100--0x1FE	16	r/w	Analogue Card EEPROM *(see § 2.2.1.3)*
0x200 to 0x27E	16	w	*Digital Inspection Lines (see §2.2.1.4)*
0x280 to 0x2EE	16	w	*Analog Inspection Lines (see §2.2.1.5)*
0x200 to 0x2FE	16	w	*Not yet allocated*
0x300—0x3FE	16	r/w	GIR Readout Setup and status register *(See § 2.2.1.5.2)*

2.2.1.1 GIR Module Control Register **:** GMCR

VME base Address : 0x10

Bit Number	Meaning when = 0	Meaning when = 1
0	Not Last Card	Last Card (use terminators)
1	Reset FIFO Disable	FIFO Reset
2	Reset DSP Disable	DSP Reset
3	Reset GIR Disable	GIR Reset
4 to 15	*Not Allocated*	*Not Allocated*

2.2.1.2 Temperature Control Register

VME Area Address : 0x40 to 0x54

Address	Function	Command
0x40	Read Temperature	0xAA
0x42	Write Temperature High	0x1
0x44	Write Temperature High	0x2
0x46	Read Temperature High	0xA1
0x48	Read Temperature Low	0xA2
0x4A	Read Counter	0xA0

0x4C	Read Slope	0xA9
0x4E	Start Convert Temperature	0xEE
0x50	Stop Convert Temperature	0x22
0x52	Write Config	0xC
0x54	Read Config	0xAC
0x56--0x5E	*Not Allocated*	

2.2.1.3 GOCCE Card EEPROM

VME Base Address : 0x100 to 0x1FC

VME Base Address	***Description***	***DATA Format***
0x100	In Read Mode this is the Man. ID	D7..D0 from XCPROM
0x102		
0x104		
0x106		
0x108	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x10a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

2.2.1.4 GOCCE Digital Inspection lines.

VME base Address : 0x200 to 0x27E

VME Address	***Bus Width***	***Rd/ Wr***	***Function***
0x200	16	r/w	Digital Inspection 1 channel select *(See §2.2.1.4.1)*
0x220	16	r/w	Digital Inspection 1 parameter Select
0x240	16	r/w	Digital Inspection 2 channel select
0x260	16	r/w	Digital Inspection 2 parameter Select

2.2.1.4.1 Digital inspection lines:

VME Address : line1 channel= 0x200, parameter = 0x220 ;
line2 channel= 0x240, parameter = 0x260

Parameters	***Data Value for channel Address***	***Data Value for Parameter Address***
Disable	*0x0*	*0xxx*
	Channel A	
DDS0	0x1	0x0
DDS1	0x1	0x1
DDS2	0x1	0x2
DDS3	0x1	0x3
DS1_0	0x1	0x4
DS1_1	0x1	0x5
DS1_2	0x1	0x6
DS1_3	0x1	0x7
PDS_Gate	0x1	0x8

PDS_Reset	0x1	0x9
FT_Sample	0x1	0xA
Val_Sample	0x1	0xB
BLR_Out	0x1	0xC
Encod_Command	0x1	0xD
ADC_CVT	0x1	0xE
ADC_Busy	0x1	0xF
ADC_Clk	0x1	0x10
ADC_Coding	0x1	0x11
End_ADC_Rdt	0x1	0x12
Timeout_Rst	0x1	0x13
CFD_Inner	0x1	0x14
DtReady	0x1	0x15
Renout	0x1	0x16
AddRam_Run0	0x1	0x17
Common Signals		
Fast Trigger	0x5	0x1
Validation	0x5	0x2
Inhibit Action	0x5	0x3
Renin	0x5	0x4
Orvalack	0x5	0x5
Startreadout	0x5	0x6
Salti Dtready	0x5	0x7
Salti Dtack	0x5	0x8
LT_RESET IN	0x5	0x9
Wr_Strobe	0x5	0xA
Resetfifo	0x5	0xB
SS_DATA	0x5	0xC
SS_CLK	0x5	0xD
SS_Strobe	0x5	0xE
SS_Link_Clk	0x5	0xF
SS_LINK_Oe	0x5	0x10
SS_Link_Ack	0x5	0x11
SS_Link_Data0	0x5	0x12
SS_Link_Data1	0x5	0x13
SS_Link_Data2	0x5	0x14
SS_Link_Data3	0x5	0x15
StopCounter	0x5	0x16
Latch_Seg_Pat	0x5	0x17
Scaler_Cnt_Ce	0x6	0x0
Wr_Scaler_SRAM	0x6	0x1
Ld_Scaler_oldVal	0x6	0x2
Incr_Scaler	0x6	0x3
Wr_Scaler	0x6	0x4

Reset_Scaler	0x6	0x8
Start_Reset_Scaler	0x6	0x6
Oe_Scaler	0x6	0x7

	Channel B	
See Upper	0x2	See Upper
	Channel C	
See Upper	0x3	See Upper
	Channel D	
See Upper	0x4	See Upper
Disable	*0x6 to 0xF*	*xx*

Parameters	***Data Value for line Address***	***Data Value for Parameter Address***
	GIR Control Lines	
Disable	0x20	0x0
	TRIGGER SIGNALS.	
Fast_Trigger	0x20	0x01
Inhibit_Action (M.T.)	0x20	0x02
Validation	0x20	0x03
Event Reject	0x20	0x04
FIFO_RENIN	0x20	0x05
	READOUT GOCCE to GIRV5	
OrValack	0x20	0x06
Conversion Dtime (coding)	0x20	0x07
StartReadout	0x20	0x08
SALTI Renin	0x20	0x09
SALTI Dtready	0x20	0x0A
SALTI Dtack	0x20	0x0B
SALTI Last Pass	0x20	0x0C
CLKWF	0x20	0x0D
ENWF	0x20	0x0E
Flag0_DSP	0x20	0x0F
Flag1_DSP	0x20	0x10
Flag2_DSP	0x20	0x11
Flag3_DSP	0x20	0x12
Irq0_DSP	0x20	0x13
Irq1_DSP	0x20	0x14
	VXI READOUT	
Inhibit_Req	0x20	0x15
AS* (VME)	0x20	0x16
DS (DS0* and DS1*) (VME)	0x20	0x17
R/W* (VME)	0x20	0x18
ModRoco	0x20	0x19
CardRenin *(From VRE)	0x20	0x1A
BLTACK (Card)	0x20	0x1B

BLTACK (Bus)	0x20	0x1C
FDTACK	0x20	0x1D
DTACK* (VME)	0x20	0x1E
Decod_Sel	0x20	0x1F
OEData_Card	0x20	0x20
LT_Reset*	0x20	0x21
ClkB_Fifo	0x20	0x22
ENB_FIFO	0x20	0x23
EmptyFIFO	0x20	0x24
Reset-Fifo	0x20	0x25
Sysclk	0x20	0x26
DSP INTERFACE		
Link_CE	0x20	0x27
DMA-Req	0x20	0x28
DMA-Grant	0x20	0x29
Link4_Start	0x20	0x2A
Link4_Ack	0x20	0x2B
Link4_Clk	0x20	0x2C
Link4_Dat0	0x20	0x2D
Link4_Dat1	0x20	0x2E
Link4_Dat2	0x20	0x2F
Link4_Dat3	0x20	0x30
Dtack_VXI	0x20	0x31
OE_DSP_Run	0x20	0x32
Event_counter_CE	0x20	0x33
Readout-Evt-Fault	0x20	0x34
Readout-Evt-Match	0x20	0x35
Wr_DSP	0x20	0x36
RD_DSP	0x20	0x37
CS_DSP	0x20	0x38
OE_ADD_DSP	0x20	0x39
MS1_DSP	0x20	0x3A
HBR_DSP	0x20	0x3B
HBG_DSP	0x20	0x3C
CS_Sram1	0x20	0x3D
WE_Sram1	0x20	0x3E
OE_Sram1	0x20	0x3F
Disable	*0x21 to 0x7E*	*xxxx*

2.2.1.5 GOCCE Analog Inspection lines.

VME base Address : 0x280 to 0x2EE

VME Address	*Bus Width*	*Rd/ Wr*	*Function*
0x280	16	r/w	Analogue Inspection 1 channel select *(See §2.2.1.5.1)*
0x2A0	16	r/w	Analogue Inspection 1 parameter Select
0x2C0	16	r/w	Analogue Inspection 2 channel select
0x2E0	16	r/w	Analogue Inspection 2 parameter Select

2.2.1.5.1 Analogue inspection lines:

VME Address for line1 : channel= 0x280, parameter = 0x2A0

for line2 : channel= 0x2C0, parameter = 0x2E0

Parameters	*Data Value for Crystal A Address*	*Data Value for Parameter Address*
Disable	*0x0*	*0xxx*
	Segment 0	
PDS 0	0x1	*0x0*
LA 0	0x1	0x1
TFA 0	0x1	0x2
In_Anal 0	0x1	0x3
	Segment 1	
PDS 1	0x1	0x4
LA 1	0x1	0x5
TFA 1	0x1	0x6
In_Anal 1	0x1	0x7
	Segment 2	
PDS 2	0x1	0x8
LA 2	0x1	0x9
TFA 2	0x1	0xA
In_Anal 2	0x1	0xB
	Segment 3	
PDS 3	0x1	0xC
LA 3	0x1	0xD
TFA 3	0x1	0xE
In_Anal 3	0x1	0xF
	Channel B	
See Upper	0x2	See Upper
	Channel C	
See Upper	0x3	See Upper
	Channel D	
See Upper	0x4	See Upper
Disable	*0x7 to 0xF*	*xx*

2.2.1.5.2 GIR Readout Control and Status register area

VME area Address : 0x300 to 0x3FE

VME Address	*Bus Width*	*Read/ Write*	*Function*
0x300	16	r/w	Event Counter Register
0x302	16	r/w	Item + Group no. for the event counter Register
0x300	32	read only	Item + Group no. + Event Counter
0x304	32	r/w	Fifo Test Access
0x308	16	r/w	DSP Control Register *(See § 2.2.1.6)*
0x30A	16	r/w	GIR Readout Control Register *(See § 2.2.1.7)*
0x30C	16	r only	Readout Status Register *(See §2.2.1.8)*
0x30E	16	r/w	Valack Timeout [1]
0x310 to 0x3FE	*N.A.*	*r/w*	*Not yet Implemented*

[1] multiple of 31.25 ns (if Clk_GIR = 33MHz); 100 <t< 4 sec. Active when bit0 of RCR is 1 *(See § 2.2.1.7)*
e.g. to have 100 us timeout write the value 0xC80 (3200).

2.2.1.6 DSP Control Register : DCR

VME area Address : 0x308

Bit	*Meaning when = 0*	*Meaning when = 1*
0	Datas Transfert from GOCCE to DSP disable	Datas Transfert from GOCCE to DSP enable [1]
1	Datas Transfert between DSP and VXI bus disable	Datas Transfert between DSP and VXI bus enable
2	DSP Link4 Transfert Disable	DSP Link4 Transfert Enable
3	DMA Test Disable	DMA Test Enable
4	Spectra process Disable	Spectra process Enable
5	Scaler process Disable	Scaler process Enable
6	GOCCE ADC SLIDING SCALE Disable	GOCCE ADC SLIDING SCALE Enable
6 to 15	*Not yet defined*	*Not yet defined*

2.2.1.7 GIRV5 Readout Control Register : RCR

VME area Address : 0x30A

Bit Nb	*Meaning when = 0*	*Meaning when = 1*
0	Disable Valack Timeout Reset	Enable Valack Timeout Reset
1	Enable Readout from GIRV5	Disable Readout from GIRV5(card is bypass)
2	Event Number Readout ON	Event Number Readout OFF
3	Qstat Disable	Qstat Enable
4	Pipeline Readout Disable	Pipeline Readout Enable
5	Common DeadTime Readout Enable	Common DeadTime Readout Disable
6	External Readout Disable	External Readout Enable
7 to 15	Not yet defined	Not yet defined

[1] Bit 0 and bit 1 are valid only if the DSP Link Transfert is enable (bit 2 =1)

2.2.1.8 GIRV5 Readout Status Register

VME base Address :0x30C

Bit Number	*Meaning when = 0*	*Meaning when = 1*
0	GIRV5 Temperature indicator is above the upper threshold	GIRV5 Temperature indicator is below the upper threshold
1	GIRV5 Temperature indicator is below the lower threshold	GIRV5 Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
9	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
10 to 15	not defined	not defined

2.2.2 Analogue Card (SALTI Area) Memory Map

This area sets up registers and Digital DACs for the 4 crystals, but the crystals are usable one by one.

VME ADDRESS (offset 0x810000)	Bus Width	Read/ Write	Function
Common AREA			
0x0800 to 0x8FC	32	R/W	common AREA *registers (see §2.2.2.2.1)*
Crystal A (0x1000 --0x1FFE)			
0x1000 to 0x103C	32	R/W	Crystal A RGI Register AREA *(see §2.2.2.2.2)*
0x1040 to 0x105C	32	R/W	Configuration & setup Area for Crystal A *(see §2.2.2.2.4)*
Crystal B (0x2000 --0x2FFE)			
0x2000 to 0x203C	32	R/W	Crystal B RGI Register AREA *(see §2.2.2.2.2)*
0x2040 to 0x205C	32	R/W	Configuration & setup Area for Crystal B *(see §2.2.2.2.4)*
Crystal C (0x3000 --0x3FFE)			
0x3000 to 0x303C	16	R/W	Crystal C RGI Register AREA *(see §2.2.2.2.2)*
0x3040 to 0x305C	32	R/W	Configuration & setup Area for Crystal C *(see §2.2.2.2.4)*
Crystal D (0x4000 --0x4FFE)			
0x4000 to 0x400E	16	R/W	Crystal D RGI Register AREA *(see §2.2.2.2.2)*
0x4040 to 0x405C	32	R/W	Configuration & setup Area for Crystal D *(see §2.2.2.2.4)*

2.2.2.1 Common Area Registers .

VME Base Address = 0x0800 +n*0x087C (n=0 to 3)

Setup Common Area	*Bus Width*	*DAC Parameter Name*
0x800	8	Common PDS Width
0x804	8	Common PDS Gate Delay
0x808	8	Common Val sample
0x80C	16	Common Watchdog Sample
0x810	16	Common Register Control (see *§2.2.2.1.1)*
0x824	16	Write SS value counter
0x828	W only	Simulate SS pulse
0x840 TO 0x87C	32	Read Scalers (*see §2.2.2.1.2)*
0x880 TO 0x8FC	32	N.Y.A.

2.2.2.1.1 Common Register Control (CRC) **0x810**:

Bit Number	*Meaning when = 0*	*Meaning when = 1*
0	Clover works as 4 independent channels	Clover works as 1 channel
1	TDC STOP FROM FT	DTD STOP from CFD_OR signal (only clover mode)
2	Enable Salti Readout	Disable Salti Readout
3	GOCCE STARTS FROM CFD INNER (Slave Mode)	GOCCE STARTS FROM GOCCE DTD (Master Mode)
4	Disable Scalers	Enable Scalers
5	Mark veto events	Reject veto events (only if CFD front edge comes inside the veto signal)
6	Disable ADC Sliding Scale	Enable ADC Sliding Scale
7	Sliding Scale value set to minimum (only if Enable =0)	Sliding Scale value set to maximum (only if Enable =0)
8	GOCCE Inhibit Request Disable	GOCCE Inhibit Request Enable
9	Latch GOCCE DTD Scalers Enable	Latch GOCCE DTD Scalers Disable
10	Reset Scalers Disable	Reset Scalers Enable
11 to 15	not defined	not defined

2.2.2.1.2 Scalers Memory Map **0x840 to 0x87c**:

Crystal A RGI Area	*Bus Width*	*Read/Write*	*Data bus 32 bits*
0x840	32	Read only	Crystal A segment 0 Scaler
0x844	32	Read only	Crystal A segment 1 Scaler
0x848	32	Read only	Crystal A segment 2 Scaler
0x84C	32	Read only	Crystal A segment 3 Scaler
0x850	32	Read only	Crystal B segment 0 Scaler
0x854	32	Read only	Crystal B segment 1 Scaler
0x858	32	Read only	Crystal B segment 2 Scaler
0x85C	32	Read only	Crystal B segment 3 Scaler
0x860	32	Read only	Crystal C segment 0 Scaler

0x864	32	Read only	Crystal C segment 1 Scaler
0x868	32	Read only	Crystal C segment 2 Scaler
0x86C	32	Read only	Crystal C segment 3 Scaler
0x870	32	Read only	Crystal D segment 0 Scaler
0x874	32	Read only	Crystal D segment 1 Scaler
0x878	32	Read only	Crystal D segment 2 Scaler
0x87C	32	Read only	Crystal D segment 3 Scaler

2.2.2.2 Register Item and Group Area for crystal A in write mode.

VME Base Address = 0x811000 +n*0x1000 (n=0 to 3)

Example given for Crystal A In write mode only bit 29 to 16 can be written.

Crystal A RGI Area	*Bus Width*	*Read/Write*	*Group and ITEM data position [29:16]*
0x1000	32	W only	ADC SEGMENT 0 Group and Item
0x1004	32	W only	ADC SEGMENT 1 Group and Item
0x1008	32	W only	ADC SEGMENT 2 Group and Item
0x100C	32	W only	ADC SEGMENT 3 Group and Item
0x1010	32	W only	TDC SEGMENT 0 Group and Item
0x1014	32	W only	TDC SEGMENT 1 Group and Item
0x1018	32	W only	TDC SEGMENT 2 Group and Item
0x101C	32	W only	TDC SEGMENT 3 Group and Item

2.2.2.3 Crystal A Data Structure in Read mode:

Example given for Crystal A In read mode only bits 31 and 30 are indicators
29 to 16 are Group & Item bits; 15 to 0 are real ADC or TDC Data and not VME DATA.

Crystal A RGI Area	**Bit 31**	**Bit 30**	**Bit 29 to 16**	**Bit 15,14**	**Bit 13 to 0**
0x1000	Not Used	VETO	ADC SEGMENT 0 G&I	Not Used	Seg0 ADC 14 bits
0x1004	Not Used	VETO	ADC SEGMENT 1 G&I	Not Used	Seg1 ADC 14 bits
0x1008	Not Used	VETO	ADC SEGMENT 2 G&I	Not Used	Seg2 ADC 14 bits
0x100C	Not Used	VETO	ADC SEGMENT 3 G&I	Not Used	Seg3 ADC 14 bits
0x1010	Not Used	VETO	TDC SEGMENT 0 G&I	Not Used	Seg0 TDC 14 bits
0x1014	Not Used	VETO	TDC SEGMENT 1 G&I	Not Used	Seg1 TDC 14 bits
0x1018	Not Used	VETO	TDC SEGMENT 2 G&I	Not Used	Seg2 TDC 14 bits
0x101c	Not Used	VETO	TDC SEGMENT 3 G&I	Not Used	Seg3 TDC 14 bits
0x1020 to 0x103C	*Not used*	*Not used*	*Not used*	*Not used*	*Not used*

2.2.2.4 Configuration & setup Area per Crystal.

VME Base Address = 0x811040 +n*0x81105C (n=0 to 3)

Example given for Crystal A.

Setup Area for Crystal A	*Bus Width*	*DAC Parameter Name*
0x1040	8	FT Sample Delay A

0x104C	16	Crystal RCR *(see § 2.2.2.2.4.1)*

2.2.2.4.1 Crystal Readout Control Register **0x81104C**:

Example given for Crystal A.

Bit Number	***Meaning when = 0***	***Meaning when = 1***
0 to 3	Disable Readout ADC Seg 0 to 3	Enable Readout ADC Seg 0 to 3
4 to 7	Disable Readout TDC Seg 0 to 3	Enable Readout TDC Seg 0 to 3
8	Disable SPARE segment (*see § 2.2.2.2.4.2*)	Enable SPARE segment (*see § 2.2.2.2.4.2*)
9	SPARE channel select 0 set to 0 (*see § 2.2.2.2.4.2*)	SPARE channel select 0 set to 1 (*see §2.2.2.2.4.2*)
10	SPARE channel select 1 set to 0 (*see § 2.2.2.2.4.2*)	SPARE channel select 1 set to 1 (*see § 2.2.2.2.4.2*)
11	Disable Crystal A LT	Enable Crystal A LT (works with GO*/STOP set to GO*)
12	Disable Crystal A TDC	Enable Crystal A TDC
13 to15	*Not Allocated*	*Not Allocated*

2.2.2.4.2 Spare segment set_up:

The spare segment is set-up as follows:

- **MUST** Set bit 8 of the CRCR to 1 to enable the spare channel FIRST.
- Set bits 9 and 10 of the CRCR to replace the bad segment by the spare segment.
- Bits 10 and 9 give the following significance:

Bit 10	**Bit 9**	**Set the spare segment**
0	**0**	Spare segment replaces segment 0
0	**1**	Spare segment replaces segment 1
1	**0**	Spare segment replaces segment 2
1	**1**	Spare segment replaces segment 3

2.2.3 *SRAM Area Address*

VME address : 0x20 0000 to 0x3F FFFC **to be defined**

SRAM Address	VME Address	Spectra
0x0+(ch nb)*0xC000	0x20 0000+(ch nb)*0x3 0000	ADC 6 Mev Data
0x4000+(ch nb)*0xC000	0x21 0000+(ch nb)*0x3 0000	ADC 20 Mev Data
0x8000+(ch nb)*0xC000	0x22 0000+(ch nb)*0x3 0000	TAC Data
0x6 0000	0x38 0000	Echelles

Ch nb : Channel Number = 0 to 7.
Spectra are coded on 14 bits (0 to 13) when GOCCE.ldr DSP program is used.
Example given for channel 0 and channel 7.

SRAM Address	VME Address	Spectra
0x0	***0x20 0000***	***ADC 6 Mev for channel 0***
0x4000	0x21 0000	ADC 20 Mev for channel 0
0x8000	0x22 0000	TAC for channel 0
0x5 4000	0x35 0000	ADC 6 Mev for channel 7
0x5 8000	0x36 0000	ADC 20 Mev for channel 7
0x5 C000	0x37 0000	TAC for channel 7

2.2.4 *DSP Area Address*

VME address : 0x40 0000 to 0x4B FFFC

DSP Address	VME Address	Data
0x0 to 0xFF	0x40 0000 to 0x40 03FC	IOP Registers *(See §2.2.4.1)*
0x2 0004 to 0x2 00FF	0x48 0010 to 0x48 03FC	Interrupt Vectors
0x2 0100 to 0x2 2FFF	0x48 0400 to 0x48 BFFC	Subroutines
0x2 3000 to 0x2 5FFF	0x48 C000 to 0x49 7FFC	Data 48 bits
0x2 6000 to 0x2 60FF	0x49 8000 to 0x49 83FC	Variables *(See §2.2.4.2)*
0x2 6100 to 0x2 FFFF	0x49 8400 to 0x4B FFFC	Data 32 bits *(See §2.2.4.3)*
0x2FFD0	0x4 BFF40	Choice Register

2.2.4.1 *IOP Registers*

VME address : 0x40 0000 to 0x40 03FC

DSP Address	VME Address	Data
0x0	0x40 0000	Syscon Register
0x2	0x40 0008	Wait Register
0x1D	0x40 0074	DMA7 Control Register
0x48 to 0x4F	0x40 0120 to 0x40 013C	DMA Channel 7 Registers *(See §2.2.4.1.1)*
0xC0 to 0xC8	0x40 0300 to 0x40 0320	Link Ports Registers *(See §2.2.4.1.2)*

2.2.4.1.1 DMA Channel 7Registers

VME address : 0x40 0120 to 0x40 013C

DSP Address	VME Address	Data
0x48	0x40 0120	II7 ➔ Internal memory address
0x49	0x40 0124	IM7 ➔ Internal memory access modifier
0x4A	0x40 0128	C7 ➔ Number of transfers remaining
0x4D	0x40 0134	EI7 ➔ External memory address
0x4E	0x40 0138	EM7 ➔ External memory access modifier
0x4F	0x40 013C	EC7 ➔ External Counter

2.2.4.1.2 Link Ports Registers

VME address : 0x40 0300 to 0x40 0320

DSP Address	VME Address	Data
0xC0	0x40 0300	LBUF0 ➔ Link buffer 0
0xC1	0x40 0304	LBUF1 ➔ Link buffer 1
0xC2	0x40 0308	LBUF2 ➔ Link buffer 2
0xC3	0x40 030C	LBUF3 ➔ Link buffer 3
0xC4	0x40 0310	LBUF4 ➔ Link buffer 4
0xC5	0x40 0314	LBUF5 ➔ Link buffer 5
0xC6	0x40 0318	LCTL ➔ Link buffer Control
0xC7	0x40 031C	LCOM ➔ Link Common control
0xC8	0x40 0320	LAR ➔ Link Assignment register

2.2.4.2 Variables

VME address : 0x49 8000 to 0x49 83FC

DSP Address	VME Address	Data
0x26000--0x2601F	0x49 8000--0x49 807C	Spectra and Scaler *(see §2.2.4.2.1)*
0x26020—0x2602F	0x49 8080--0x49 80BC	Power Supplies Inspection *(see §2.2.4.2.2)*

2.2.4.2.1 Spectra and Scaler

DSP Address	VME Address	Data
0x26000	0x49 8000	Subroutine number
0x26001	0x49 8004	First Item number
0x26002	0x49 8008	Event number
0x26003	0x49 800C	Data number per event
0x26004	0x49 8010	Error counter on item number
0x26005	0x49 8014	Error counter on data number

2.2.4.2.2 Power Supplies Inspection

DSP Address	VME Address	Data

0x26020	0x49 8080	Multiplexer Input Number
0x26021	0x49 8084	Coding Resolution

2.2.4.3 Data 32 bits

VME address : 0x49 8400 to 0x4B FFFC **to be defined**

DSP Address	VME Address	Data
0x26100--0x261FF	0x49 8400—0x49 87FC	Spectra and Scaler *(see §2.2.4.3.1)*
0x26200--0x266FF	0x49 8800--0x49 9BFC	Power Supplies Inspection *(see §2.2.4.3.2)*

2.2.4.3.1 Spectra and Scaler

DSP Address	VME Address	Data
0x26100 + (ch nb)*0x3	0x49 8400 + (ch nb)*0xC	ADC 6 Mev Data
0x26101 + (ch nb)*0x3	0x49 8404 + (ch nb)*0xC	ADC 20 Mev Data
0x26102 + (ch nb)*0x3	0x49 8408 + (ch nb)*0xC	TAC Data

Ch nb : Channel Number = 0 to 7.
Example given for channel 0 and channel 7.

DSP Address	VME Address	Data
0x26100	0x49 8000	ADC 6 Mev Data for channel 0
0x26101	0x49 8004	ADC 20 Mev Data for channel 0
0x26102	0x49 8008	TAC Data for channel 0
0x26103	0x49 800C	ADC 6 Mev Data for channel 7
0x26104	0x49 8010	ADC 20 Mev Data for channel 7
0x26105	0x49 8014	TAC Data for channel 7

2.2.4.3.2 Power Supplies Inspection.

DSP Address	VME Address	Data
0x26200—0x26206	0x49 8800	Multiplexer input selection
0x26207—0x26214	0x49 881C	Power Supplies Table Reference
0x26215—0x2621B	0x49 8854	Power Supplies Average
0x2621C—0x26222	0x49 8870	Deviation
0x26223—0x26622	0x49 888C	ADC Data

2.2.4.4 Choice register

Bit Number	Meaning when = 0	Meaning when = 1
0	DMA between SALTI16 and GIRDSP disable	DMA between SALTI16 and GIRDSP enable
1	DMA between GIRDSP and FIFO disable	DMA between GIRDSP and FIFO enable
2	*Not allocated*	*Not allocated*
3	Totpeak function disable	Totpeak function enable
4	Reset DSP internal memory disable	Reset DSP internal memory enable
5	Mux_ADC coding and scanning disable	Mux_ADC coding and scanning enable
6	*POLE_ZERO (not yet installed)*	*POLE_ZERO (not yet installed)*
7	Reset DSP internal and external memory disable	Reset DSP internal and external memory enable
8	Spectra process disable	Spectra process enable

9	Scaler process disable	Scaler process enable
10	GOCCE ADC SLIDING SCALE Disable	GOCCE ADC SLIDING SCALE Enable
12	Mux_ADC coding and spectra disable	Mux_ADC coding and spectra enable
13 to 15	*not defined*	*not defined*

2.3 SPACE Area Address.

VME Area Address : 0x1000000 to 0x2FFFFC

VME Memory Addresses	*Function*
Channel A SPACE Area : 0x1000000 to 0x17FFFFC):	
0x1000000 to 0x11FFFFC	SPACE A External Memory Area Address
0x1200000 to 0x13FFFFC	SPACE A DSP1 Area Address
0x1400000 to 0x15FFFFC	SPACE A DSP2 Area Address
0x1600000 to 0x17FFFFC	SPACE A DSP3 Area Address
Channel B SPACE Area : 0x1800000 to 0x1FFFFFC	
0x1800000 to 0x19FFFFC	SPACE B External Memory Area Address
0x1A00000 to 0x1BFFFFC	SPACE B DSP1 Area Address
0x1C00000 to 0x1DFFFFC	SPACE B DSP2 Area Address
0x1E00000 to 0x1FFFFFC	SPACE B DSP3 Area Address
Channel C SPACE Area : 0x2000000 to 0x27FFFFC	
0x2000000 to 0x21FFFFC	SPACE C External Memory Area Address
0x2200000 to 0x23FFFFC	SPACE C DSP1 Area Address
0x2400000 to 0x25FFFFC	SPACE C DSP2 Area Address
0x2600000 to 0x27FFFFC	SPACE C DSP3 Area Address
Channel D SPACE Area : 0x2800000 to 0x2FFFFFC	
0x2800000 to 0x29FFFFC	SPACE D External Memory Area Address
0x2A00000 to 0x2BFFFFC	SPACE D DSP1 Area Address
0x2C00000 to 0x2DFFFFC	SPACE D DSP2 Area Address
0x2E00000 to 0x2FFFFFC	SPACE D DSP3 Area Address