TDR Pattern Register User Manual

Contents

Appendices

Refers to pcb 25/9275A.

1. Introduction

The Pattern Register is a single width VME module designed to operate in the GREAT TDR environment. There are two groups of 16 inputs, A and B. The purpose of the module is to register the changes on the inputs, and send a timestamped 16 bit pattern to the Data Acquisition system via a SHARC link. The timestamp refers to the selected edge of the input. The two groups can be set to one of three specific digital interface types. Fast NIM, Differential ECL, and Single ended ECL.

The Pattern input is operated as two Groups, each in one of three operating modes. All the pattern inputs are AND'ed with a programmable mask bit, which allows individual bits to be disabled, for example where one input is firing in noise. GroupA can be pulse stretched under computer control.

1. Gated Group:
   The front edge of the Group Gate input will latch the master 100MHz counter and all inputs which are active at any time during the Group Gate will be included in the pattern. The pattern and timestamp is output at the end of the Gate.

2. Individual inputs:
   a) The 16 pattern inputs of the Group are individually sampled on every clock. Those that became active since the previous clock generate a timestamp along with a label to say which of the 16 inputs caused the timestamp.
   b) In this mode the user may choose (under computer control) to AND the input with the Group Gate.
   c) GroupA AND GroupB. This mode uses the GroupA and GroupB inputs to provide 16 bits of co-incidence pattern. A timestamp is generated when the input from GroupA AND GroupB are true to-gether.

The Timestamp is based on a counter incremented by a 100Mhz clock and kept in synchronism with the rest of the TDR system by the SYNC pulse provided by the GREAT TDR system Metronome module.

The Pattern Register is designed to operate at an average input rate of 10Khz per input. The maximum burst rate into one input is 10Mhz. The minimum input pulse width for reliable operation is 50ns, however much smaller input pulses can be registered.

The following documents will help in understanding the terms discussed in this manual. They can be found at the Nuclear Physics Group web site : http://npg.dl.ac.uk

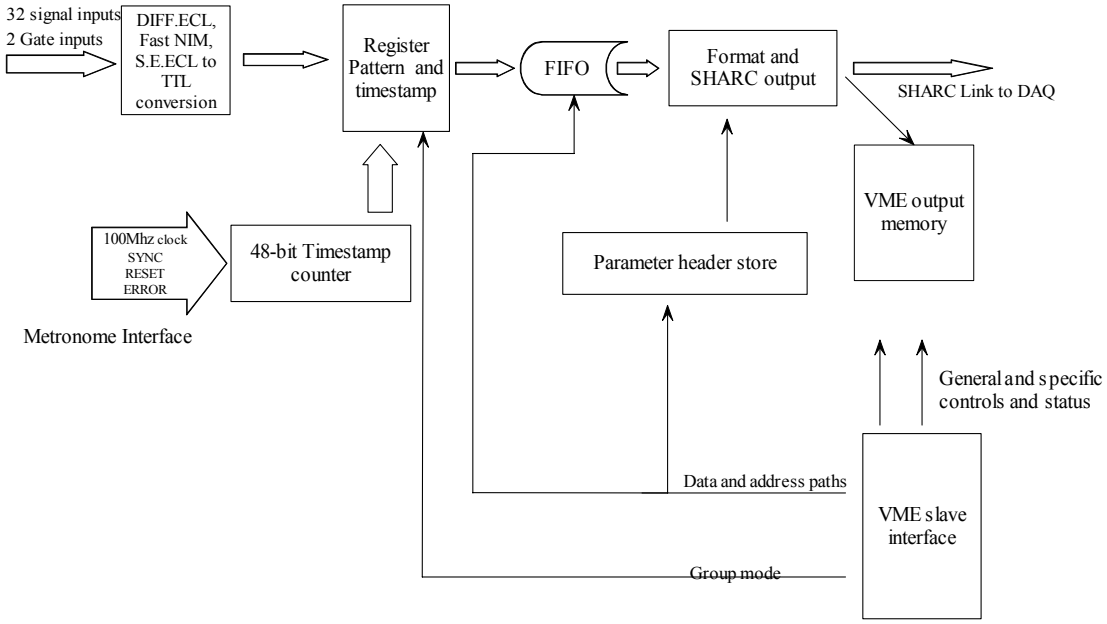
EDOC502 The GREAT Triggerless Total Data Readout Method (IEEE TNS, VOL. 48, NO. 3, JUNE 2001)
EDOC503 The GREAT 32 Channel Peak Sensing ADC : User Manual
EDOC504 The GREAT data format.
EDOC507 The GREAT TDR system Error recovery, and experiment timing
EDOC511 Metronome User Manual Version6 (C1100)

2. Function

The function of the module is carried out by two Altera FPGA devices programmed at power-up from serial EPROMs. There is an LED for each FPGA which is lit when the programming has completed successfully.
The user of the module must decide the interface type for each of the 16 inputs in the two Groups. The jumpers must then be set accordingly. Refer to section 3.b and appendix A for setting the different interface choices.
The inputs to be registered are chosen by using the MIDAS interface window. See appendix C for an example of the window for the Pattern Register.
The sense of each input can be inverted, controlled via MIDAS, prior to being applied to the Register timestamp logic. This allows the user to decide which edge of the input signal causes the timestamp. It is always the rising edge of the input that is timestamped.
As mentioned in the introduction each group operates in one of two modes. The mode must be selected via the MIDAS interface.
To operate the module must be connected to a TDR Metronome output, or a similar source of 100Mhz, and SYNC pulses.

a. Block Diagram

The block diagram shows the path of data from input signal to SHARC output.



b. VME interface specification

The Pattern Register is an A32/D32 slave. The interface will respond to accesses made using D16, and D08, however they will not return the correct values.
The Pattern Register occupies 2^{16} bytes in A32 memory space. The address of location 0 is specified by jumpers set on the pcb. See section 3.a and appendix A for setting the address base.

c. SHARC interface data format.

The Pattern Register outputs two 32 bit words for every Item. An Item can be for an input transition from GroupA, or GroupB, a SYNC pulse, a flow control Pause, or a flow control Resume. Refer to EDOC504 for more information about the bit allocation of these two words.
Here is an outline of the Item format extracted from the EDOC.

Group Pattern Data format

31	30	29	28	27 to 16	15 to 0
1	1	0	0	Data Source Ident,	Pattern data
31 to 28				27 to 0	
0				Time Stamp 27:0	

Other Information.

31	30	29 to 24	23 to 20	19 to 0
1	0	Module Number	Information Code	Information Field
31 to 28			27 to 0	
0			Time Stamp 27:0	

The Module number identifies the source of the information.

The Information codes used in the Pattern Register are as follows:

Information Type	Code	Information Field Definition
Undefined Data	0	
Pause Timestamp	2	Timestamp bits 47 : 28
Resume Timestamp	3	Timestamp bits 47 : 28
SYNC100 Timestamp	4	Timestamp bits 47 : 28

3. Setting Up

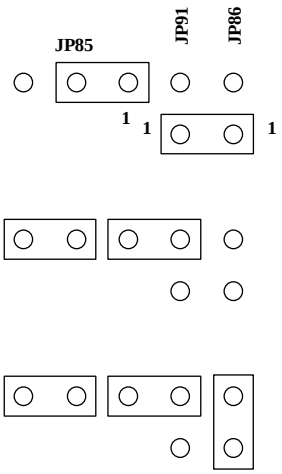
a. VME Address Jumpers.

Refer to the picture of the module shown in Appendix A. The VME address jumpers are in two, eight jumper blocks at the middle of the top of the pcb. The address of location 0 of the module address space is specified by placing, or not, shorting links ion the jumpers. Placing a shorting link on a jumper will select that address bit to be seen as a logic 0.
For example to select address 0x80000000 for the base address, shorting links should be placed on every jumper except the one for A31. (This is the jumper at the left most end of the row, as indicated by the white writing).

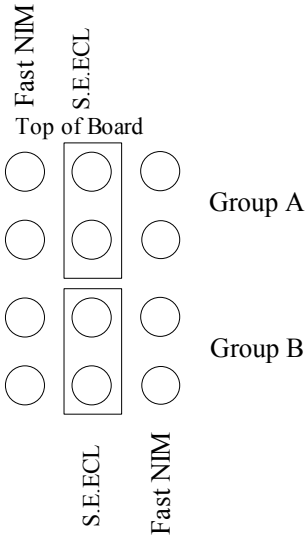
b. Input Selection

Each of the 32 inputs can be selected to interface to signals of one of three types. Fast NIM, Differential ECL, and Single ended ECL. The following jumper diagrams show how to select each of the possible types.
Differential ECL does not require a specific reference voltage selected, but the Fast NIM, and Single Ended ECL do.

It is important to note that all the inputs for a group should be set to the same interface type. Failu re to do this will resu lt in incor rect ref erence v oltages bein g used, and unpredictable register operation ;-)



Input Selection Jumper Positions



Voltage Reference selection

When connecting to the front panel inputs use the following signal allocations with the 34 pin IDC connectors.
Input 0 in *Differential ECL* mode pin1 is the +ve input, and pin 2 the –ve. This carries on through the connector with Input 15 on pin 31 for +ve an d pin 32 for –ve. Pins 33, and 34 are not connected on both Group A and B input connectors.
Input 0 in *Fast NIM*, and *Single Ended ECL* mode pin1 is the Signal input, and pin 2 the GND. This carries on through the conne ctor with Input 15 on pin 31 for Signal input and pin 32 for GND. Pins 33, and 34 are not connected on both Group A and B input connectors.

4. Operation

The mode of operation applies to all the inputs of a Group. The mode is selected using the MIDAS interface.
The operation of the m odule is handled by the MIDAS interface, and would norm ally only require the user to select the inputs, their polarity, and the Group Modes. If the module is to be operated in an environm ent not controlled by MIDAS, then a m uch deeper understanding of the m odule function is requ ired than is co vered in this version of the user manual. Contact the author for help .
To operate within the MIDAS environm ent the m odule must be configured in the VME address space, an d the correct Group In terface jumper settings selected for th e inputs. The module is entered in the VME configuration table accessed via the VME control window. This allows the MIDAS to set-up and control the module.
With the SHARC link connected to the TDR Collato r processor, and the Me tronome interface connected the module will be set-up by the MIDAS with initial values in all the registers, and valid entries for the module readout identifiers.
Use the Experiment Control window Setup and Go buttons.
The mode of operation of the two groups of inputs is controlled by m enu selection in the MIDAS interface. The tab le b elow gives th e valid m odes. A# refers to the inp ut number within the group A.

Value	Mode name	Comment
0	Single: input(A/B)# AND Gate(A/B)	
1	Single: input(A/B)#	
2	Gated Group	
4	Single : A# AND B# AND GateA	Group A input only
5	Single : A# AND B#	Group A input only
6	Gated Group : A# AND B#	Group A input only
12	Single : Stretched A# AND B# AND GateA	Group A input only
13	Single : Stretched A# AND B#	Group A input only

a. Single Input mode.

In this mode each input operates alone. Each input must be enabled via the MIDAS interface. The Group Gate input can be selected to be ANDed with the inputs. This selection operates for the whole of a group.

b. Gated Group.

The front edge of the Group Gate input will latch the master 100MHz counter and all inputs which are active at any time during the Group Gate will be included in the pattern. The Group Gate input is a Fast NIM signal.

c. GroupA AND GroupB, or Using the TDR Pattern Register for providing timed suppression data.

The purpose is to combine the VETO signal from the Eurogam Phase 1 BGO detectors and electronics with a Ge CFD to give a timestamped data item indicating the co-incidence of the two signals.

The Pattern Register 32 inputs are allocated as two groups of 16. Group B is used for the Single Ended ECL VETO signals from the BGO electronics, and Group A is used for the Fast NIM Ge CFDs from the LeCroy CFD modules.

The Ge CFD signals are stretched in the Pattern Register to align them with the slower VETO signals. Fig 1 shows when the timestamped Item is generated for a single CFD and VETO.

It should be noted that a timestamped Item will be generated for <u>every</u> coincidence between the VETO, and CFD. Fig 2 shows how this can occur during multiple VETOs

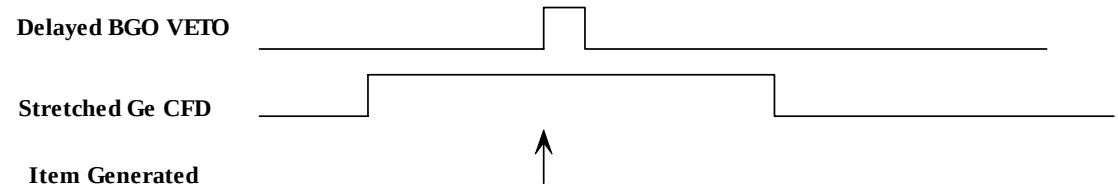


Fig 1: Single CFD Aligned with VETO

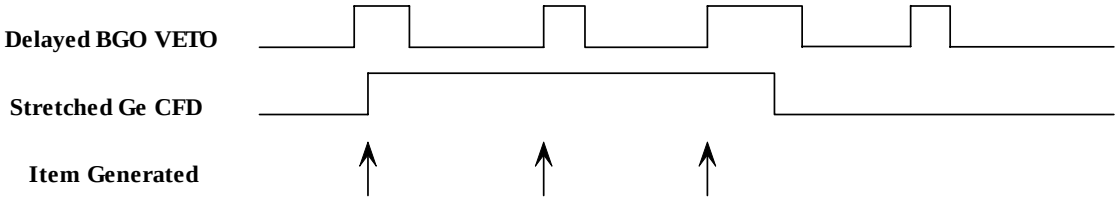


Fig 2: Multiple VETOs align with one CFD

When setting up for an experiment it will be necessary to check the alignment of the Ge CFD and VETO signals, as well as the width of the CFD.
Logic Inspection Lines are provided in each Pattern Register for this job.
The width of the CFD output pulse will also affect the number of co-incidences.

5. Software Interface

Access to the registers on the Pattern Register are via the VME bus interface using A32/D32 commands. The registers are defined in the table in Appendix E at the end of this document. For further information about register function contact the author via email.
The normal method of control is via the MIDAS control window. The module should be initialized after power-up with registers set as follows.

6. Front Panel Interface

The front panel layout is shown in a diagram in Appendix B.
The connections are detailed in the following Tables.

SHARC Link.

Pin	Function	Source
1	Clock	Pattern Register
2	Acknowledge	VME Processor
3	GND	
4	Data 0	Pattern Register
5	Data 1	Pattern Register
6	Data 2	Pattern Register
7	Data 3	Pattern Register
8	GND	

Group Inputs (A/B) Differential ECL Interface

Pin	Function	Pin	Function
1	Input 0 +ve	2	Input 0 -ve
3	Input 1 +ve	4	Input 1 –ve
….		….	
31	Input 15 +ve	31	Input 15 –ve
33	No Connection	34	No Connection

Group Inputs (A/B) Single Ended ECL Interface

Pin	Function	Pin	Function
1	Input 0	2	Ground
3	Input 1	4	Ground
….		….	
31	Input 15	31	Ground
33	No Connection	34	No Connection

Group Inputs (A/B) Fast NIM Interface

Pin	Function	Pin	Function
1	Input 0	2	Ground
3	Input 1	4	Ground
….		….	
31	Input 15	31	Ground
33	No Connection	34	No Connection

7. Logic Inspection Signal examples

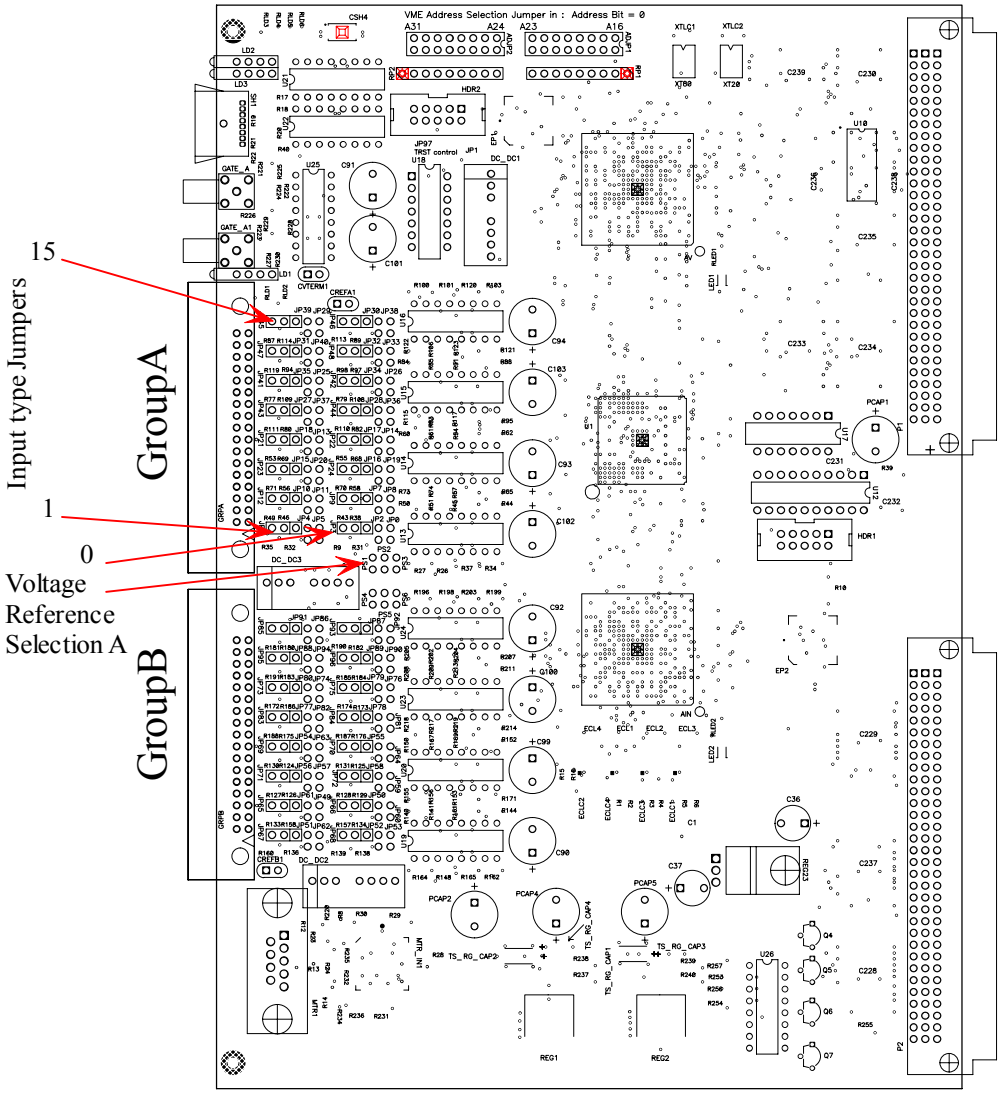
During normal use of the module the inputs, and Gate signals are the most likely to be required. The examples show which edge of the signal as seen through the Inspection Lines generates the Timestamp.

8. What can stop the module working, or Error management.

1. Lost Track.
   Refer to the block diagram in section 2.a. There is a FIFO between the timestamping input stage, and the formatting and SHARC link stage. The data is placed into the FIFO with a four bit count to keep track of the data through the FIFO. If the data coming through the FIFO is not in step, then the module will stop working, the Lost Track LED will light, and the relevant bit is set in the status register. The operation of the module is re-started by a system STOP/SETUP/GO action.
2. Using the wrong edge of the input for timing.

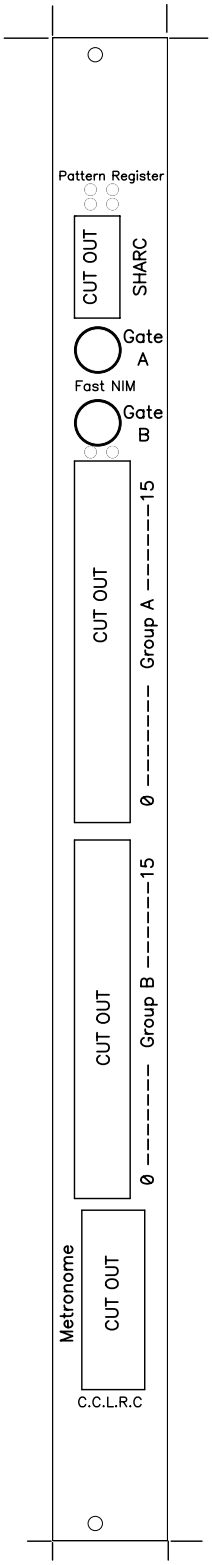
3. Appendix A Jumper Layout

VME Address Jumpers



Outline of the Pattern Register for location of Jumpers.

Appendix B Front Panel Layout



Front Panel for 25/9275
All Dimensions in mm
All hole sizes are for finished size.

Appendix C MIDAS control window.

Appendix D Logic Inspection signal examples.

Appendix E Software Register definitions.

Register definitions:

Address offset Hexadecimal	Name	Function
0	Module Control	0 : ignore track. 1= Ignore the tracking data when reading FIFO 1 : SHARC enable. 1 = Enable SHARC link readout of the FIFO. 2 : Reset FIFO 3 : STARX enable. 1= Enable STARX to reset FIFO. 4 : Soft Reset input chip. 5 => 15 : registered data, but no action. 16 => 31 : always return 0.
4	Module Status	0 : interrupt. 1 : lost track. 2 : FIFO Half full. 3 => 31 : Always return 0.
8	Interrupt Control	0 => 7 : Interrupt vector. 8 => 10: Select IRQ line to drive on VME bus. 11 => 15 : registered data, but no action. 16 => 31 : always return 0.
C	Interrupt Select	0 => 3 : Select Interrupt source. 0: Lost Track. 1: FIFO half full. 2 => 15 not defined. 4: Method. 0 = Edge triggered, 1 = Level Triggered 5: Edge. 0 = Rising edge, 1 = falling edge. 6: Level. 0 = High Level, 1 = Low level. 7: Enable 0 = Disabled, 1 = Enabled. 8 => 15 : registered data, but no action. 16 => 31 : always return 0.
10	Read FIFO	0 => 31: FIFO output data.
14	Read Tracking Registers	0 => 3 : Readout track Counter 4 => 7 : Track number from FIFO. 8 => 11 : ID track number from last ID word. 12 => 15 : Track number from last Time stamp. 16 => 31: 0.
18	FIFO Flags	All these flags are active low. 0 : Almost full. 7 spaces remaining. 1 : Almost empty. 7 words written. 2 : Half full. 131,072 words written 3 : Empty. 4 : Full. 262,144 words written 5 => 31 : 0.
1C	Spare Bus	0 => 31 : VME chip end of Spare connections between the two Alteras
100	Group A input enable	Bits 15 => 0 enable an input when set.

104	Group A Invert	Bits 15 => 0 invert the logic of the input bit when set.
108	Group A mode	Selects registered/free/free & Gate mode. 0: Free Transition Mode. 1= enabled. 1: Registered Mode. 1 = enabled. 2: AND mode (CFD + VETO) 1= enabled. 3: Stretch input pulses. 1 = enabled.
110	Group A Stretch value	Bits 3 => 0 select the pulse stretch value in steps of 50ns.
200	Group B input enable	Bits 15 => 0 enable an input when set.
204	Group B Invert	Bits 15 => 0 invert the logic of the input bit when set.
208	Group B mode	Selects registered/free/free & Gate mode.
300	Inspection Line 0	Selects the signal source
304	Inspection Line 1	Selects the signal source
308	Inspection Line 2	Selects the signal source
30C	Inspection Line 3	Selects the signal source
400	Input Chip control	0 : Reset input FIFOs 1 : Count Enable. 1 = Enable Time stamp counter. 2 : SYNC error reset. 3 : SYNC to Error (STARY) connect. 4 : No effect, but registered. 5 : Run Enable. 1 = Enable input of SYNC, and Data to the FIFOs. 6 => 15 : registered data, but no action. 16 => 31 : always return 0.
404	Input Status	Timestamp errors and others (NYI !!!)
500	Time FIFO LS	0 => 31 : Time stamp bits 0 => 31.
504	Time FIFO MS	0 => 15 : Timestamp bits 32 => 47. 16 => 31 : 0.
508	Time FIFO word count	0 => 8 : Number of words in the Timestamp FIFO
50C		
510	Group A fifo data	0 => 15 : Group A Pattern 16 => 31 : 0
514		
518	Group A fifo word count	0 => 8 : Number of words in the Group A FIFO 16 => 31 : 0
51C		
520	Group B fifo data	0 => 15 : Group B Pattern 16 => 31 : 0
524		
528	Group B fifo word count	0 => 8 : Number of words in the Group B FIFO 16 => 31 : 0
52C		
530	Type fifo data	0 => 7 : Event type data. 8 => 31 : 0.
534		
538	Type fifo word count	0 => 8 : Number of words in the Event type FIFO 16 => 31 : 0
53C		
540	Group A Ident	0 => 31 : Ident for Group A pattern.
544	Group B Ident	0 => 31 : Ident for Group B pattern.
548	SYNC Ident	0 => 31 : Ident for SYNC.
54C	Pause Ident	0 => 31 : Ident for Pause.
550	Resume Ident	0 => 31 : Ident for Resume.
554	Undefined Ident	0 => 31 : Ident for Undefined.

558	Write to FIFO.	0 => 31 : write to FIFO.
55C		
560	FIFO flags	0 : Group A FIFO empty 1 : Group A FIFO full 2 : Group B FIFO empty 3 : Group B FIFO full 4 : Control FIFO empty 5 : Control FIFO full. 6 : Timestamp FIFO empty 7 : Timestamp FIFO full. 8 : External FIFO almost full. 9 : External FIFO full. 10 => 31 : 0
600	Load Timestamp	Load a new value into the Timestamp counter for loading at a re-sync SYNC pulse. 0 => 31 : Data for new Timestamp 16 => 47 value. A write to this register sets the Re_SYNC enable.
700	Spare bus read	0 => 31 : Input chip end of Spare connections between the two Alteras.

Appendix F. Logic Inspection Line signal selection.

Logic Inspection Line Signal selection. This inform ation is provided for completeness, it is not intended f or a us er to need to vie w the m ajority of thes e signals.

Code	Signal Name	Description
0 => 1F	Disconnected	Allows other units to drive the line.
20 => 2F	Group A inputs 0 => 15	Input monitors for Group A.
30 => 3F	Group B inputs 0 => 15	Input monitors for Group B.
40	Group B Hit	Group B Pattern hit.
41	Group B End	Group B Gated mode End signal
42	Gate A	Group A Gate input.
43	Gate B	Group B Gate input.
44	Sync pulse	Sync detected 10nS pulse
45	Sync error	Sync error flag
46	Aneb	Output of Timestamp sync comparator
47	Re-load window	Window a fter S YNC pulse during which a re-load can occur.
48	Load stamp	Re-load pu lse. Loads the new value into the Timestamp counter
49	Load Enable	Indicates a re-load has been programmed.
4A	Time FIFO read	FIFO read request signal for the Timestamp FIFO
4B	Time FIFO full	Flag
4C	Time FIFO empty	Flag
4D	Group A FIFO read	FIFO read request signal for the Group A FIFO
4E	Group A FIFO	Flag

	full	
4F	Group A FIFO empty	Flag
50	Group B FIFO read	FIFO read request signal for the Group B FIFO
51	Group B FIFO full	Flag
52	Group B FIFO empty	Flag
53	Time FIFO write	FIFO write request for the Timestamp FIFO
54	Group A FIFO write	FIFO write request for the Group A FIFO
55	Group B FIFO write	FIFO write request for the Group B FIFO
56	Pause	Pause signal
57	Resume	Resume signal
58	Type FIFO read	FIFO read request signal for the Type FIFO
59	Type FIFO full	Flag
5A	Type FIFO empty	Flag
5B	SYNC	SYNC pulse from the Metronome
5C	STARX	STARX (Reset) from the Metronome
5D	Out of step	Internal FIFOs are out of step ???????
5E	Ext FIFO write clock	FIFO Write clock to the external FIFO
5F	Ext FIFO write	FIFO Write request to the external FIFO
60	Ext FIFO almost full	Flag (active low)
61	Ext FIFO full	Flag (active low)
62	Group A Hit	Group A Pattern hit.
63	Group A End	Group A Gated mode End signal
70 => 7F	Group A stretched 0 => 15	The Stretched inputs for Group A.
80	Loadreg	Load signal, enables reg isters when selected to load data
81	Chip select	Active to select vme access to the input chip
82	Asn	VME address strobe
83	DS0n	VME Data strobe 0
84	DS1n	VME Data strobe 1
85		
86	DTACK	VME data acknowledge
87	STARX	
88	Iackn	VME Interrupt acknowledge cycle identifier
89	Irq1	Interrupt line
8a	Irq2	Interrupt line
8b	Irq3	Interrupt line
8c	Irq4	Interrupt line

8d	Irq5	Interrupt line
8e	Irq6	Interrupt line
8f	Irq7	Interrupt line
90	Iackinn	Interrupt cycle chain token in
91	Iackoutn	Interrupt cycle chain token out
92	Sharc_clock	SHARC bus clock pulses.
93	Sharc_ack	SHARC bus acknowledge
94	Sharc data0	SHARC data bit
95	Sharc data1	
96	Sharc data2	
97	Sharc data3	
98 – 9f	NYI	
A0	Fifo pafn	FIFO programmable almost full
A1	Fifo paen	FIFO programmable almost empty
A2	Fifo hfn	FIFO Half empty
A3	Fifo ffn	FIFO full
A4	Fifo efn	FIFO empty
A5	Fifo erclk	Fifo erclk ?????
A6	Fifo erenn	Fifo erenn ????
A7	Fifo rclk	Fifo read clock
A8	Fifo rcsn	Fifo read chip select
A9	Fifo renn	Fifo read enable
Aa	Fifo oen	Fifo output enable
Ab	Fifo prsn	Fifo partial reset
Ac	Fifo mrsn	Fifo master reset
Ad	Fifo ready	Fifo data has been read, and is ready for use
Ae	Fifo rdreq	Request from sharc software for a fifo read
Af	Vme req	Request from vme for a read of fifo data
B0	Lost track	Output of the track comparison system ?