AIDA FEE specification

The FEE will interface the AIDA ASIC to the Data acquisition software, providing facility for control and event gathering. The ASIC will connect to the detector.
Timing of events will be based on the BuTiS distributed clock. A signal will be provided for other parts of the experiment based on the OR of all the channel discriminators within the ASICs. Communication with the FEE for data transfer and control will be using an ethernet interface.

The FEE consists of a number of unit modules. Each module will contain sufficient equipment to support 8 ASICs and hence 128 detector channels. The module will contain a number of FPGAs to carry out the tasks.

Inputs to the module comprise 128 connections to a Silicon strip detector. Outputs from the module are blocks of Time ordered events. Events are formed from ASIC processed signals or VHDL and Flash ADC processed signals.

Constraints on the FEE.

The FEE must occupy boards with an 8cm maximum dimension at the interface with the detectors.
Each 8cm width must contain sufficient ASICs and acquisition electronics for 128 channels.
The required Implant rate into the Detector is 10Khz. The FEE is based on this figure with a maximum Implant rate per detector strip of 1Khz.

Proposed layout

The Aida FEE module (AFEM) for 128 channels will be split between two boards. Each board will contain the required electronics for 64 channels. Boards are called AFE64.
Each AFE64 will connect to the Detector along half of the 8cm length. The ASICs will be mounted on a mezzanine to allow for easy replacement in case of channel failure.
The two AFE64s are mechanically attached with one mirrored beneath the other.

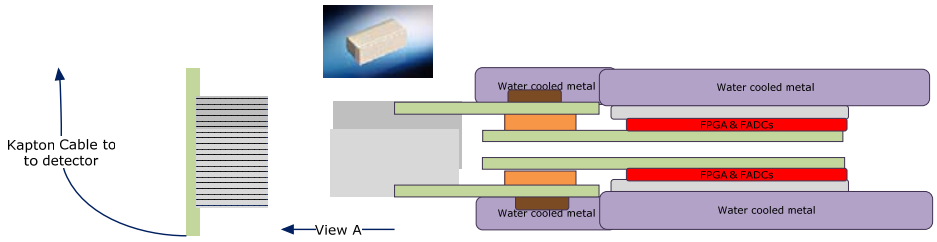


Diagram (above) of the AFE64 boards as they would fit in the vertical plane. The thin grey rectangles are heat conductive foam pads which conform to the component outlines and conduct the heat to the water cooled metalwork. The green is pcb, the orange is a Samtec 80 pin connector with a 2.3mm height and the dark brown is the ASIC. The

connections to the detector will be on the mezzanine boards to the left and to the acquisition network computers and BUTIS on the right. These are not shown.

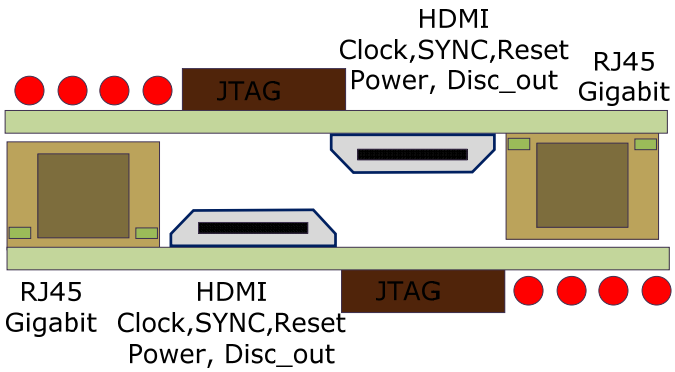
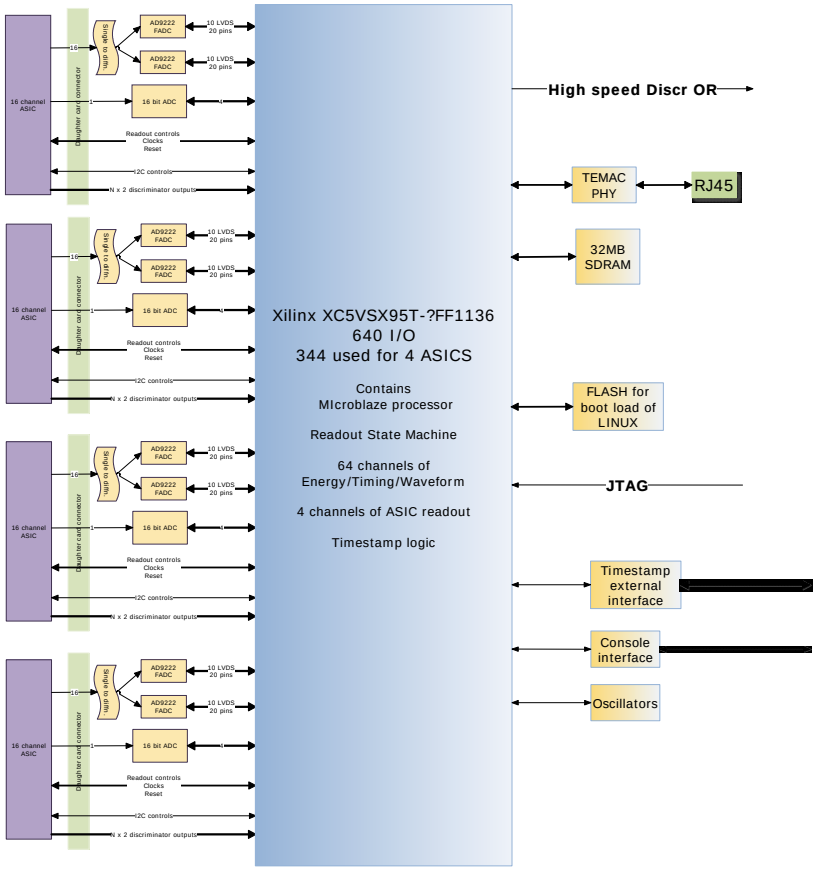


Diagram (above) of the connectors at the end of the AFEM showing the HDMI connector(for 200Mhz clock, SYNC, Reset, power , and fast trigger OR) , the JTAG connector, the Gigabit RJ45, and the comfort LEDs.



AIDA - FEE (64) - ASIC to DAQ block diagram

AFE64 functional blocks

- **Mezzanine** with four ASICs mounted. Connecting to the detector using an ERNI hard 2mm pitch connector (914794) mounted underneath the mezzanine board and extending over the edge of the AFE64. The detector is connected, via Kapton cable, to an intermediate board (AFEIB) mounted in the AFE crate (AFECT) with the ERNI mating connector (103753). Each AFECT has two connectors to handle the 128 channels of one AFEM.

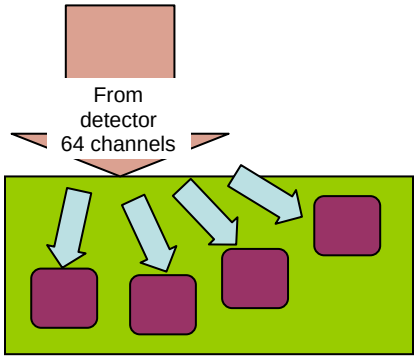
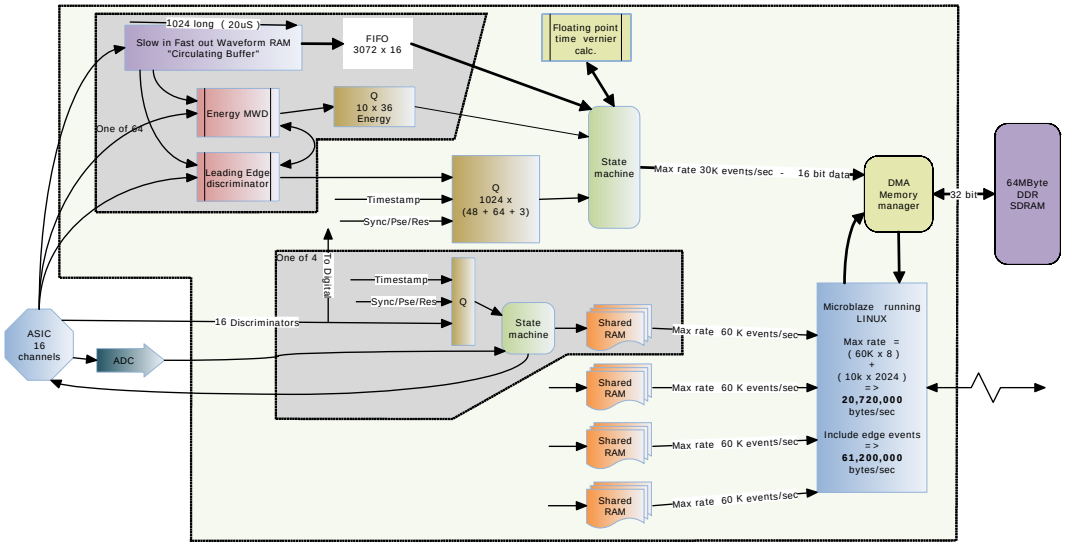


Diagram (above) illustrates the connection between the ASIC mezzanine and the detector.

- **FPGA board** which contains :-
  - FPGA with VHDL and processor code which are stored in flash memories and loaded into the FPGA on power-up.
  - Analogue to digital conversion
  - Analogue buffers
  - Power supplies
  - Processor peripherals
  - Clock interface.
  - Connections for external interfaces.
- **VHDL functions :-**
  - **Microblaze** soft processor running LINUX to handle transfer of data to Acquisition computers and for control of the AFE64.
  - **Detector digital readout** to collect data from the waveforms digitised by the FADC for each channel and process them using MWD and discriminator packages. Events will be stored in intermediate memory and transferred to processor memory under control of a state machine.
  - **Detector analogue readout** to collect data from the ASIC using the multiplexed analogue output and controls.
  - **Timestamp** used to provide a time relationship between events and coordinated by the external clock system. Timestamps are queued in a fifo for each of the detector readout blocks and used to generate event data.

- **Internal Data Transfer** state machines to read data from the Event memories and transfer it to the processor memory for transfer to the acquisition computers. The access to the processor memory is made using DMA channels in the memory control interface. In the case of large volumes of data, lossless compression will be applied.
- **Floating point Time vernier** calculations are carried out during the Readout transfer of the Digital waveforms. The results are then added to the end of the event.



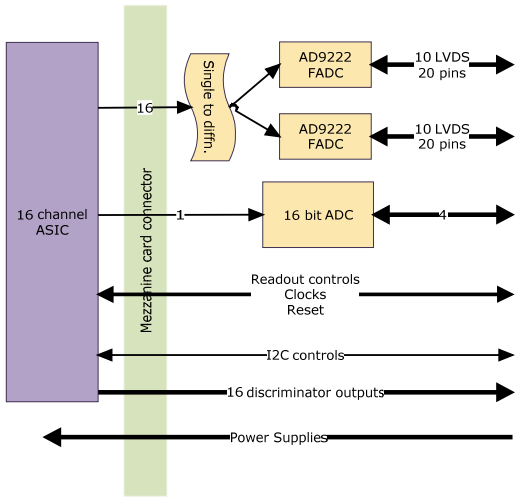
Block diagram of the VHDL structure of the FPGA showing data paths and rates.

- **Processor functions:-** *(The operating system is LINUX)*
  - **Control of the AFE64** including setting up the ASICS and monitoring the status of the equipment in the module.
  - **Slow control** interface with the run control and setup softwarae in the acquisition computers. TCP/IP will be used over the Gbit link.
  - **Transfer of data packets** containing time ordered event data to the acquisition computers and handling any link problems. UDP will be used over the Gbit link.
  - **Initialisation** from power-up with automatic data link calibration between the FADC and the FPGA fabric. Initial communications with and setup of the ASICs will occur.

- **Processor external peripherals :-** *(mostly copied from a Xilinx Virtex5 development board used for software development so interchange between development and AFE64 is easy.)*
  - **Gigabit Phy** interfacing between the internal Gbit interface and the RJ45 connector.
  - **SDRAM** devices to make a 32 bit memory of 64MB or such a value as fits with the devices available.
  - **Flash memory** to contain the software for the Microblaze. This memory will be accessible for re-loading using the Microblaze or the JTAG interface.

- **RS232** converter chip to translate the local signals to the correct levels for the console.
- **LED** drivers for the information LEDs.
- **Temperature and Voltage measurement** modules interfaced using an addressed bit serial interface.
- **ID memory** which contains a programmable value to allow software to generate an individual MAC address. This is a 128 byte EEPROM accessed via an I^2C interface.

- **ASIC acquisition and control** requires 54 connections per ASIC.
  - **I^2C** – bit serial register access route between the FEE and the ASIC. – 2 signals. Clock and bidirectional data.
  - **Channel discriminator output** to create timestamps of activity. – 16 logic signals.
  - **Channel preamp outputs** for Digital signal processing. – 16 analogue signals with a single reference voltage.
  - **Discriminator OR** – LVDS Logic signal (jitter spec 400pS RMS) to give 1ns timing. – 2 signals.
  - **Multiplexed analogue** – The output of the readout analog multiplexor. 1 signal with reference.
  - **Readout information** – Logic signals to indicate which channel is on the multiplexed analogue and allow handshaking between the ASIC control and the readout logic in the FPGA. 7 logic signals.
  - **Readout control** – Controls the output of multiplexed analogue. 4 signals including a RESET.
  - **Calibration register control** – Logic signals to control the calibration connections in the ASIC. A step voltage will inject the calibration charge to the selected channels. 3 Logic and one analogue.



AIDA - FEE - Support connections and parts for one chip

The main components used.

One Xilinx Virtex5 FPGA will be used on each AFE64 to control and collect events for four ASICs and to communicate with the Acquisition computers. The device chosen will have a common footprint with other Virtex5s in the product range should a different capability be required in future (i.e. more BRAM/DSP/Processor blocks).

Each preamplifier channel for Detector digital readout will be buffered using single to differential driver designed for interfacing to the flash ADC. Eight Detector digital readout channels will share one AD9252 14bit flash ADC. Each device contains eight convertors with continuous data readout from each convertor over separate 350Mhz DDR serial links. The 350Mhz clock and a frame signal are provided for the FPGA to convert the data to parallel form.

Each Detector analogue readout channel will be converted using an AD7686 (or equivalent) which is a small footprint serial output 500Ksps 16 bit ADC.

Data Transfer system design information *(refer to the VHDL block diagram)*

Detector analogue readout (one per ASIC)

Module event rates are based on the following :

- Expect 6 events per implant at 10Khz.
  - 5 from implantation
  - 1 from decay
- Use “flip-flop” memory for event store.
- Each event is two 32 bit words. (GREAT format)
- Use 4 BRAMs as two blocks of 1024 x 32
- 512 items can be stored which is 512/6 = 85 implants. Thus the maximum time that can be stored is 2 x 85 x 100uS = 17mS.
- The time to readout one store at a 32bit bus speed of 100Mhz is 1024 x 10nS = 10uS
- All four stores can be read in 40uS.
- A CPU tick of 1mS will be fine

Detector digital readout (one per 64 channels)

Module event rates are based on the following :

- Expect 3 events per implant at 10Khz. All in different channels - on average.
  - 2 from edge of the implant.
  - 1 from decay.
- Event comprises Energy, Time , Ident, Quality, and Waveform (size is WS).
- Waveform is 20uS>WS>2uS
- Incoming data is stored in a “circulating buffer”.
- When LE discriminator and MWD logic agree signal is sent to the Timestamp Queue.
- Energy and quality is sent to its Channel Queue and when available waveform is sent to a FIFO.

AFE64 data volume

- Contribution from Detector analogue readout
    - 6 events per implant at 10khz => 60K events per second
    - Two 32 bit words per event => 8 bytes.
    - Total => 480KB/sec
- Contribution from Detector digital readout
    - 3 events per implant at 10Khz => 30K events per second.
    - Worst case : 20us waveform + four 32 bit words => 2032 bytes.
    - Total => 60,960KB/sec. (Too much for the current design and funds so compression and/or waveform length reduction would have to be used at full implant rate.)
    - Compression of the waveform 2 to 3 times and a reduction to 10us waveform => 532bytes x 30,000 => 15,960KB/sec.
- Total Data volume => 16,440KB/sec.

NB This does not map linearly to give the data volume for the full AIDA system.

Clock distribution and Discriminator OR return.

The BuTiS clock and associated system control and synchronisation signals will be distributed using an HDMI cable format from a central resource module. The Discriminator OR signal from the ASICs will be sent using the same cable. During system configuration the use of some of these connections will change to allow the timing of the clocks to be aligned.

Power and cooling

Power will be sent to the module using the HDMI connector using 24volts. The internal power supplies will be derived from the 24Volts using a mixture of DC-DC convertors and linear regulators. There is no High Voltage on this module.
Cooling of the module will be implemented using water cooled metal and heat conducting insulating material. The AFECT (crate) will contain water cooled metal plates which can be clamped to the modules when they are inserted. The modules will conduct heat from the electronics using metal structures and heat conducting foam. The temperature of the equipment will be maintained at 20 Centigrade to ensure moisture cannot condense on the electronics. (or such suitable temperature for local experiment conditions).
The mechanical structure holding the two AFE64 modules together to form the AFEM will be defined once the full power requirements of the module is established and the cooling structure of the AFECT is defined. At present an estimate is **100W** per AFEM. However the VHDL design and clock rates will have a major impact on this figure. The prototype will use forced air cooling instead of water cooled plates.

Grounding

The modules will share a local ground at the AFECT. If required this can be connected to Detector ground. The Gbit network will be optically isolated from the Acquisition computers after network router/switch boxes. All other equipment with connections to the

FEE system will use the same local ground. Connections to equipment on the local ground MUST be isolated either using optical or inductive techniques.