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AIDA FEE rate calculations.

The FEE module contains the electronics to readout 128 strips from silicon detectors. There are two FPGAs each handling 64 strips via 4 ASICs each. The ASIC contains a high and a low gain path for each strip. Each path contains discriminators, shaping amplifiers and control logic to find the peak energy and multiplex it to a single output for ADC conversion and readout.

The FEE contains 128 low energy digitised paths where the signal from the ASIC preamp is output to flash ADCs unless the event is a high energy event in which case the signal is supressed from the ASIC.

The Silicon detectors are arranged in slices of three detectors with X strips joined across all three. The number of slices can vary up to 16 in a detector.

The detector is designed to receive implanted particles which subsequently decay by alpha or beta or proton decay.

The particle rate is set at 10,000 per second.

The particle will pass through a number of slices before implantation. Average of this is a half.

As the particle passes through a slice a high energy event occurs with a typical interaction with 5 strips in X and 5 strips in Y.

As the particle is implanted a high energy event occurs with a typical interaction with 5 strips in X and 5 strips in Y.

When the particle decays there are typically 3 decays. Alpha and Proton decays will typically interact with just one slice and beta decays will interact with typically half of the slices. These interactions will be low energy events readout both from the low energy path in the ASIC and the digital path into the FPGA. Low energy interactions typically involve one strip in X and one strip in Y.

Consider the events generated by a particle in the whole detector:

N = number of slices.
Passage events = N/2 * (5 + 5)
Decay events (beta as worst case) = N/2*(1 + 1) * 3

The high energy events require data to define the strip (2 bytes) , the Energy (2 bytes), and the Time of interaction (4 bytes). Total 8 bytes.

Low Energy events require the same as for high energy events to readout the ASIC and an additional amount for the digital path. Digital path requires 20us of waveform data (16bits for 1000 words : 2000 bytes), Energy from MWD (4 bytes), Time of interaction (4 bytes), time of interaction vernier (2 bytes) , and strip ID (2 bytes). Total 2012 bytes.

So for the typical particle there are N/2*(5+5) High Energy events requiring 8 bytes each and N/2*(1 + 1) * 3 low Energy events requiring 2012 + 8 bytes each.

The total data required per particle is typically N * 40 + N * 2020 * 3 bytes => N*6100 bytes.

Thus for the 10K/sec particle rate (PR) => N*6100 *10000 => N * 61,000,000 bytes/sec

In a 16 slice detector this gives **976Mbytes/sec** from the whole detector.

FPGA Maximum rate

Consider the maximum data rate required in a single FPGA using the same calculations. The FPGA used in the X plane will receive the most events.

So for the High Energy events the slice rate in X will be the particle rate in 5 strips. => PR * 5 => 50,000 events/sec.

The Low Energy event slice rate in X will be the particle rate in one strip => PR => 10,000 events/sec..

So an FPGA has to handle

> 50,000 + 10,000 ASIC readouts/sec
> 10,000 Digital path readouts/sec.
> Total data is 10,000 * 2012 + 60,000 * 8 bytes/sec => **21Mbytes/sec**

A digital path will be designed to cope with 1,000 events/sec as a maximum rate with 5 (initial thought) contiguous events as a maximum.

The above calculations will be used to design the data transfer parameters for the whole system and the readout paths within one FPGA.

Implantation edge effect on rate

If however the edge strips of the implantation look like low energy events they will be readout of the digital channel.
So an FPGA now has to handle

> 50,000 + 10,000 ASIC readouts/sec
> 30,000 Digital path readouts/sec.
> Total data is 30,000 * 2012 + 60,000 * 8 bytes/sec => **61Mbytes/sec**

The system rate is now given by :-
The total data required per particle is typically
N * 40 + N * 2020 * 3 + N * 2012 * 2 bytes => N*10124 bytes.

Thus for the 10K/sec particle rate (PR) => N*10124 *10000 => N * 101,240,000 bytes/sec

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In a 16 slice detector this gives **1,620 Mbytes/sec** from the whole detector.