Using the HDMI_Divider.

The HDMI_Divider module receives the clock and data signal from the white-rabbit source at CN1 and divides the clock according to the selection made with the three jumpers at “Divide_select” header. Output is from Port 1.

The header pin 1 is top left and pin 2 is top right with the board in the orientation shown. Jumpers are numbered J0(pins 1&2) , J1(pins 3&4) , J2(pins 5&6). The following table gives the divisions that can be obtained. The FEE64s require 50MHz.

	J2	J1	J0
No Division	0	X	X
Divide by 2	1	0	0
Divide by 4	1	0	1
Divide by 8	1	1	0
Divide by 16	1	1	1