

## x724 DPP-PHA Registers Description

Register name	Address	Mode
Record Length	0x1n20, 0x8020	R/W
Number of Events per Aggregate	0x1n34, 0x8034	R/W
Pre Trigger	0x1n38, 0x8038	R/W
Data Flush	0x1n3C, 0x803C	W
Channel n Stop Acquisition	0x1n40 (channel n), 0x8040 (all channels, write only)	R/W
RC-CR2 Smoothing Factor	0x1n54 (channel n), 0x8054 (all channels, write only)	R/W
Input Rise Time	0x1n58 (channel n), 0x8058 (all channels, write only)	R/W
Trapezoid Rise Time	0x1n5C (channel n), 0x805C (all channels, write only)	R/W
Trapezoid Flat Top	0x1n60 (channel n), 0x8060 (all channels, write only)	R/W
Peaking Time	0x1n64 (channel n), 0x8064 (all channels, write only)	R/W
Decay Time	0x1n68 (channel n), 0x8068 (all channels, write only)	R/W
Trigger Threshold	0x1n6C (channel n), 0x806C (all channels, write only)	R/W
Rise Time Validation Window	0x1n70 (channel n), 0x8070 (all channels, write only)	R/W
Trigger Hold-Off Width	0x1n74, 0x8074	R/W
Peak Hold-Off	0x1n78 (channel n), 0x8078 (all channels, write only)	R/W
Baseline Hold-Off	0x1n7C (channel n), 0x807C (all channels, write only)	R/W
DPP Algorithm Control	0x1n80, 0x8080	R/W
Shaped Trigger Width	0x1n84 (channel n), 0x8084 (all channels, write only)	R/W
Channel n Status	0x1n88	R
AMC Firmware Revision	0x1n8C	R
DC Offset	0x1n98, 0x8098	R/W
Input Dynamic Range	0x1nB4 (channel n), 0x80B4 (all channels, write only)	R/W
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W
Aggregate Organization	0x800C	R/W
Acquisition Control	0x8100	R/W
Acquisition Status	0x8104	R
Software Trigger	0x8108	W
Global Trigger Mask	0x810C	R/W
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W
LVDS I/O Data	0x8118	R/W
Front Panel I/O Control	0x811C	R/W
Channel Enable Mask	0x8120	R/W
ROC FPGA Firmware Revision	0x8124	R
Set Monitor DAC	0x8138	R/W

Software Clock Sync	0x813C	W
Board Info	0x8140	R
Monitor DAC Mode	0x8144	R/W
Event Size	0x814C	R
Time Bomb Downcounter	0x8158	R
Memory Buffer Almost Full Level	0x816C	R/W
Run/Start/Stop Delay	0x8170	R/W
Board Failure Status	0x8178	R
Disable External Trigger	0x817C	R/W
Trigger Validation Mask	0x8180+(4n)	R/W
Front Panel LVDS I/O New Features	0x81A0	R/W
Readout Control	0xEF00	R/W
Readout Status	0xEF04	R
Board ID	0xEF08	R/W
MCST Base Address and Control	0xEF0C	R/W
Relocation Address	0xEF10	R/W
Interrupt Status/ID	0xEF14	R/W
Interrupt Event Number	0xEF18	R/W
Aggregate Number per BLT	0xEF1C	R/W
Scratch	0xEF20	R/W
Software Reset	0xEF24	W
Software Clear	0xEF28	W
Configuration Reload	0xEF34	W
Configuration ROM Checksum	0xF000	R
Configuration ROM Checksum Length BYTE 2	0xF004	R
Configuration ROM Checksum Length BYTE 1	0xF008	R
Configuration ROM Checksum Length BYTE 0	0xF00C	R
Configuration ROM Constant BYTE 2	0xF010	R
Configuration ROM Constant BYTE 1	0xF014	R
Configuration ROM Constant BYTE 0	0xF018	R
Configuration ROM C Code	0xF01C	R
Configuration ROM R Code	0xF020	R
Configuration ROM IEEE OUI BYTE 2	0xF024	R
Configuration ROM IEEE OUI BYTE 1	0xF028	R
Configuration ROM IEEE OUI BYTE 0	0xF02C	R
Configuration ROM Board Version	0xF030	R
Configuration ROM Board Form Factor	0xF034	R
Configuration ROM Board ID BYTE 1	0xF038	R
Configuration ROM Board ID BYTE 0	0xF03C	R
Configuration ROM PCB Revision BYTE 3	0xF040	R
Configuration ROM PCB Revision BYTE 2	0xF044	R

Configuration ROM PCB Revision BYTE 1	0xF048	R
Configuration ROM PCB Revision BYTE 0	0xF04C	R
Configuration ROM FLASH Type	0xF050	R
Configuration ROM Board Serial Number BYTE 1	0xF080	R
Configuration ROM Board Serial Number BYTE 0	0xF084	R
Configuration ROM VCXO Type	0xF088	R

## Record Length (0x1n20, 0x8020, R/W, I)

Sets the record length for the waveform acquisition

Bit	Description
[15:0]	Number of samples (Ns) for the waveform acquisition, where the Record Length = $Ns \times 2$ (e.g.: write $Ns = 10$ to acquire 20 samples). Multiply this value by the sampling rate (10 ns) to get the record length value in ns.

## Number of Events per Aggregate (0x1n34, 0x8034, R/W, I)

The board has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffer, called "aggregates", whose number of events can be programmed by this register.

Bit	Description
[9:0]	Number of events per aggregate. Maximum value is 1023.
[31:10]	Reserved

## Pre Trigger (0x1n38, 0x8038, R/W, I)

Sets the Pre Trigger for the waveform acquisition. Once the event triggers, the digital samples are delayed by the pre trigger number of samples, to ensure that the waveform is completely acquired.

Bit	Description
[9:0]	Number of samples $Ns$ for the Pre Trigger width, where Pre Trigger = $Ns \times 2$ . The value is expressed in steps of sampling frequency, 10 ns.
[31:10]	Reserved

## Data Flush (0x1n3C, 0x803C, W, I)

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Bit	Description
[31:0]	In case of incomplete aggregates (buffers) due to a stop acquisition, or to a small trigger rate and large buffer size, a write access to this register performs a read of the incomplete buffer.

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## Channel n Stop Acquisition (0x1n40 (channel n), 0x8040 (all channels, write only), R/W, )

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Bit	Description
[0]	Performs the stop acquisition for channel n. While the run is common among all channels of the board, it is possible to perform the stop/start acquisition for a single channel. Options are: 0: run; 1: stop.
[31: 1]	Reserved

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## RC-CR2 Smoothing Factor (0x1n54 (channel n), 0x8054 (all channels, write only), R/W, )

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Bit	Description
[5: 0]	Number of samples to be averaged in the generation of the RC-CR2 signal. Write (in hex) the corresponding number of samples. Options are: 0x1: 1 sample; 0x2: 2 samples; 0x4: 4 samples; 0x8: 8 samples; 0x10: 16 samples; 0x20: 32 samples.
[31: 6]	Reserved

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## Input Rise Time (0x1n58 (channel n), 0x8058 (all channels, write only), R/W, )

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Bit	Description
[7: 0]	Rise Time of the Input pulse, expressed in sampling clock units (10 ns)
[31: 8]	Reserved

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## Trapezoid Rise Time (0x1n5C (channel n), 0x805C (all channels, write only), R/W, )

Set the Trapezoid Rise Time width, i.e. the Trapezoid Shaping Time.

Note: the sum of the Trapezoid Shaping Time and Trapezoid Flat Top (0x1n60) should not exceed 15 us times the Decimation value for x724 series, 8 us for x730 series.

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Bit	Description
[9: 0]	Trapezoid Rise Time value expressed in sampling clock unit (10 ns). This value corresponds to the trapezoid shaping time.
[31: 10]	Reserved

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## Trapezoid Flat Top (0x1n60 (channel n), 0x8060 (all channels, write only), R/W, )

Sets the Trapezoid Flat Top width.

Note: the sum of the Trapezoid Rise Time (0x1n5C) and Trapezoid Flat Top should not exceed 15 us times the Decimation value for x724 series, 8 us for x730 series.

Bit	Description
[9: 0]	Trapezoid Flat Top duration expressed in sampling clock unit (10 ns).
[31: 10]	Reserved

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## Peaking Time (0x1n64 (channel n), 0x8064 (all channels, write only), R/W, )

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Bit	Description
[10: 0]	Peaking Time: Position on the flat top region where the samples for the calculation of the peak height are taken. The peaking time is referred to the trigger or to the trigger validation signal according to the trigger mode. Check the User Manual for further details. The peaking time is expressed in sampling clock unit (10 ns).
[31: 11]	Reserved

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## Decay Time (0x1n68 (channel n), 0x8068 (all channels, write only), R/W, )

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Bit	Description
[15: 0]	Exponential Decay Time, corresponds to the time constant of the input tail. The correct setting of this parameter is useful for the pole-zero cancellation of the trapezoid. The decay time is expressed in sampling clock unit (10 ns).
[31: 16]	Reserved

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## Trigger Threshold (0x1n6C (channel n), 0x806C (all channels, write only), R/W, )

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Bit	Description
[13: 0]	Trigger Threshold value expressed in LSB unit. The threshold is referred to the RC-CR2 signal. The trigger fires at the zero crossing of the RC-CR2 signal itself.
[31: 14]	Reserved

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## Rise Time Validation Window (0x1n70 (channel n), 0x8070 (all channels, write only), R/W, )

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Bit	Description
[9: 0]	Rise Time Validation Window width used by the rise time discriminator (RTD). The zero crossing of RC-CR2 signal must occur before the end of the Rise Time Validation Window. The width is expressed in sampling clock unit. When 0, the RTD is disabled.
[31: 10]	Reserved

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## Trigger Hold-Off Width (0x1n74, 0x8074 , R/W, I)

The Trigger Hold-Off is a logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration

Bit	Description
[5: 0]	Set the Trigger Hold-Off width in steps of 8 times the sampling clock unit (10 ns). Triggers are inhibited for the overall Trigger Hold-Off duration.
[31: 6]	Reserved

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## Peak Hold-Off (0x1n78 (channel n), 0x8078 (all channels, write only), R/W, )

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Bit	Description
[7: 0]	Peak Hold-off extension: This parameter defines how close must be two trapezoids in order to be considered piled-up. Zero corresponds to the case where the flat top of one trapezoid starts exactly at the end of the flat top of the previous one. The peak hold-off extension is expressed in steps of 8 times the sampling clock unit (10 ns).
[31: 8]	Reserved

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## Baseline Hold-Off (0x1n7C (channel n), 0x807C (all channels, write only), R/W, )

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Bit	Description
[7: 0]	Baseline Hold-off extension: Defines how long the baseline is kept frozen beyond the end of the trapezoid; after that time, the baseline starts to be calculated again but it might take some time (depending on the number of samples for the baseline mean) to recover. The baseline hold-off extension is expressed in steps of the sampling clock unit (10 ns).
[31: 8]	Reserved

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## DPP Algorithm Control (0x1n80, 0x8080, R/W, I)

Management of the DPP algorithm features

Bit	Description
[5:0]	<p>Trapezoid Rescaling: The trapezoid evaluated inside the FPGA can be represented as a 48 bit number, where the number of most significant bits depends on the trapezoid rise time (k) and on the input signal decay time (M). 15 bits over 48 are reported by the board as the energy value.</p> <p>The trapezoid rescaling N defines how many LSB are thrown away (i.e. right shift) before the trapezoid height is saved in the memory buffer. This correspond to a division by <math>2^N</math>. In normal conditions, the value of N is such that <math>2^N \leq M \cdot k &lt; 2^{N+1}</math>.</p>
[7:6]	Reserved
[9:8]	<p>Decimation: the input signal samples can be averaged within the number of samples defined by the decimation. This has the analogous effect as reducing the sampling frequency of the board. Options are:</p> <p>00: Decimation disabled; 01: 2 samples (50 MSps); 10: 4 samples (25 MSps); 11: 8 samples (12.5 MSps).</p>
[11:10]	<p>Digital Gain, the input samples are digitally multiplied by the Digital Gain value. Options are:</p> <p>00: Digital Gain = 1; 01: Digital Gain = 2 (only with decimation <math>\geq 2</math> samples); 10: Digital Gain = 4 (only with decimation <math>\geq 4</math> samples); 11: Digital Gain = 8 (only with decimation = 8 samples).</p>
[13:12]	<p>Peak Mean: corresponds to the number of samples for the averaging window of the trapezoid height calculation.</p> <p>Note: for a correct energy calculation the Peak Mean should be contained in the flat region of the Trapezoid Flat Top. Options are:</p> <p>00: 1 sample; 01: 4 samples; 10: 16 samples; 11: 64 samples.</p>
[14]	Reserved
[15]	<p>Enable Spike Rejection. When this bit is enabled triggers are inhibited until the "Input Rise Time" duration is reached (register 0x1n58). In case of noisy signals this feature is quite useful to avoid triggering on spikes on the rise time of the RC-CR2 signal, which do not corresponds to real signals. This feature allows also the use to set lower values of the trigger threshold. Options are:</p> <p>0: disabled; 1: enabled.</p>
[16]	<p>Invert Input: Individual setting for the input signal inversion. The DPP-PHA algorithm is designed to work with positive signals. The input signal polarity can be inverted inside the FPGA before applying the DPP algorithm. Options are:</p> <p>0: positive polarity; 1: negative polarity.</p>
[17]	<p>Trigger on RC-CR or RC-CR2 signal. The trigger usually fires on the zero crossing of the RC-CR2 signal. For fast input signal it is possible to set the trigger on the zero crossing of the RC-CR signal (which becomes bipolar for fast signals). Options are:</p> <p>0: Trigger on RC-CR2; 1: Trigger on RC-CR.</p>

[19: 18]	<p>Trigger Mode. Options are:</p> <p>00: Normal mode. Each channel can self-trigger independently from the other channels;</p> <p>01: Neighbour mode. Each channel triggers also when either the previous or the consecutive channel triggers as well;</p> <p>10: Coincidence mode. Each channel saves the event only when a validation signal occurs in coincidence within its shaped trigger;</p> <p>11: Anti-coincidence mode. Each channel saves the event only when a validation signal occurs in anti-coincidence within its shaped trigger.</p>
[22: 20]	<p>Baseline averaging window: number of samples for the baseline average calculation. Options are:</p> <p>000: the baseline is not evaluated, and the energy values are not subtracted by the baseline;</p> <p>001: 16 samples;</p> <p>010: 64 samples;</p> <p>011: 256 samples;</p> <p>100: 1024 samples;</p> <p>101: 4096 samples;</p> <p>110: 16384 samples;</p> <p>111: reserved.</p>
[23]	Reserved
[24]	<p>Disable Self Trigger. If disabled the self-trigger is still propagated to the mother board for coincidence logic and TRG-OUT front panel connector, though it is not used by the channel to acquire the event. Options are:</p> <p>0: self-trigger enabled;</p> <p>1: self-trigger disabled.</p>
[25]	<p>Fake Event in case of Time Reset signal from GPI (S-IN in case of VME form factor). Set this bit to 1 to enable a fake-event saving in case of reset from GPI. The fake event is tagged from bit[3] of the EXTRAS word of the Channel Aggregate data format. Check the User Manual for further details. Options are:</p> <p>0: disabled;</p> <p>1: enabled.</p>
[26]	<p>Fake Event in case of Time Stamp roll over. Set this bit to 1 to enable a fake-event saving in case of internal time stamp roll over. The fake event is tagged from bit[3] of the EXTRAS word of the Channel Aggregate data format. Check the User Manual for further details. Options are:</p> <p>0: disabled;</p> <p>1: enabled.</p>
[27]	<p>Energy calculation in case piled-up events. When a pile-up occurs the board returns energy = 0; set this bit if you want the energy evaluated also for piled-up events. Events are flagged as pile-up though bit[16] of the last word of the Channel Aggregate data format. The energy value is anyway not corrected. Check the User Manual for further details. Options are:</p> <p>0: disabled;</p> <p>1: enabled.</p>
[31: 29]	Reserved

## Shaped Trigger Width (0x1n84 (channel n), 0x8084 (all channels, write only), R/W, I)

Set the number of samples for the Shaped Trigger width. The Shaped Trigger is a logic signal generated by a channel in correspondence with its local self-trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Bit	Description
[7: 0]	Set the number of samples for the Shaped Trigger width. This is useful both to set the width of the TRG-OUT signal, and to set the coincidence time window width.
[31: 8]	Reserved



## Channel n Status (0x1n88, R, I)

This register contains the status information of channel n.

Bit	Description
[1: 0]	Reserved
[2]	If 1, the SPI bus is not available, therefore it is not possible to access registers 0x1nB4 and 0x1nB8
[31: 3]	Reserved

## AMC Firmware Revision (0x1n8C, R, I)

Returns the DPP firmware revision (mezzanine level).

To control the mother board firmware revision see register 0x8124.

For example: if the register value is 0xC3218303:

- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

Bit	Description
[7: 0]	Firmware revision number
[15: 8]	Firmware DPP code. Each DPP firmware has a unique code.
[19: 16]	Build Day (lower digit)
[23: 20]	Build Day (upper digit)
[27: 24]	Build Month. For example: 3 means March, 12 is December.
[31: 28]	Build Year. For example: 0 means 2000, 12 means 2012

## DC Offset (0x1n98, 0x8098, R/W, I)

Adjust the DC Offset level for channel n to exploit the full input dynamic range of the digitizer. A write access is in broadcast mode at 0x8098 is supported to set the same value for all the channels at once.

Bit	Description
[15: 0]	DC Offset value in DAC LSB unit. Since the DAC ranges over 16 bits, while the ADC is over 14 bits, write the desired value multiplied by 4.
[31: 16]	Reserved

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## Input Dynamic Range (0x1nB4 (channel n), 0x80B4 (all channels, write only), R/W, )

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Bit	Description
[3:0]	Select the channel input range for x781 series. Options are: 0x5: 0.3 Vpp; 0x6: 1.0 Vpp; 0x9: 3.0 Vpp; 0xA: 10 Vpp.
[31:4]	Reserved

## Board Configuration (0x8000, 0x8004 (BitSet), 0x8008 (BitClear), R/W, C)

This register contains general settings for the board configuration.

Bit	Description
[0]	Reserved: must be 0.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1.
[7: 5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[9]	Reserved: must be 0
[10]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. The two analog probes can be selected from bits[13:12] and bits[15:14] respectively.
[13:12]	Analog Probe 1: Selects which signal is associated to the Analog trace 1 in the readout data. Options are: 00: Input; 01: RC-CR (input 1st derivate); 10: RC-CR2 (input 2nd derivate); 11: Trapezoid (output of the trapezoid filter).
[15:14]	Analog Probe 2: Selects which signal is associated to the Analog trace 2 in the readout data. Options are: 00: Input; 01: Threshold, which is referred to the RC-CR2 signal; 10: Trapezoid – Baseline; 11: Baseline (of the trapezoid).
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length 0x1n20 register. According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Energy Mode: When enabled, the height of the trapezoid (which corresponds to the peak amplitude of the pulses) is saved into the event data (last word of the event). Options are: 0: Energy Mode disabled. 1: Energy Mode enabled.
[18]	Time Stamp Recording: When enabled, the time stamp of the event (which corresponds to the zero crossing in the RC-CR2 timing filter) is saved into the event data (first word of the event). 0: Time Stamp recording disabled. 1: Time Stamp recording enabled.
[19]	Reserved: must be 0

[23: 20]	<p>Digital Virtual Probe 1: when the mixed (or oscilloscope) mode is enabled, the following digital virtual probes can be selected. Check the User Manual for further details.</p> <p>0000: shows the RT Discrimination Width;</p> <p>0001: "Armed", digital input showing where the RC-CR2 crosses the Threshold;</p> <p>0010: "Peak Run", starts with the trigger and last for the whole event;</p> <p>0011: "Peak Abort", corresponds to the time interval when the energy calculation is disabled due to the pile-up event;</p> <p>0100: "Peaking", shows where the energy is calculated;</p> <p>0101: "Trg Validation Win", digital input showing the trigger validation acceptance window TVAW;</p> <p>0110: "BSL Holdoff", shows the baseline hold-off parameter;</p> <p>0111: "TRG Holdoff", shows the trigger hold-off parameter;</p> <p>1000: "Trg Validation", shows the trigger validation signal TRG_VAL ;</p> <p>1001: "Acq Veto", this is 1 when either the input signal is saturated or the memory board is full.</p>
[24]	Enable FORMAT Word in the aggregate data. Must be 1.
[31: 25]	Reserved

## Aggregate Organization (0x800C, R/W, C)

The internal memory of the digitizer can be divided into a programmable number of aggregates, where each aggregate contains a specific number of events. This register defines how many aggregates can be contained in the memory.

Note: this register must not be modified while the acquisition is running.

Bit	Description																				
[3: 0]	<p>Aggregate Organization Nb: the number of aggregates is equal to <math>N_{aggr} = 2^{Nb}</math>. The corresponding values of Nb and N_aggr are:</p> <p>Nb: N_aggr</p> <table> <tr><td>0x0 - 0x1:</td><td>Not used</td></tr> <tr><td>0x2</td><td>: 4</td></tr> <tr><td>0x3</td><td>: 8</td></tr> <tr><td>0x4</td><td>: 16</td></tr> <tr><td>0x5</td><td>: 32</td></tr> <tr><td>0x6</td><td>: 64</td></tr> <tr><td>0x7</td><td>: 128</td></tr> <tr><td>0x8</td><td>: 256</td></tr> <tr><td>0x9</td><td>: 512</td></tr> <tr><td>0xA</td><td>: 1024</td></tr> </table>	0x0 - 0x1:	Not used	0x2	: 4	0x3	: 8	0x4	: 16	0x5	: 32	0x6	: 64	0x7	: 128	0x8	: 256	0x9	: 512	0xA	: 1024
0x0 - 0x1:	Not used																				
0x2	: 4																				
0x3	: 8																				
0x4	: 16																				
0x5	: 32																				
0x6	: 64																				
0x7	: 128																				
0x8	: 256																				
0x9	: 512																				
0xA	: 1024																				
[31: 4]	Reserved: must be 0																				

## Acquisition Control (0x8100, R/W, C)

This register permits configuring the acquisition settings.

Bit	Description
[1:0]	Start/Stop Mode Selection. Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using Front Panel I/O Control register, 0x811C, and Front Panel LVDS I/O New Features register, 0x81A0.
[2]	Acquisition Start/Arm. When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition; the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Trigger Counting Mode Selection. Options are: 0 = only accepted triggers are counted; 1 = all triggers are counted.
[4]	Reserved.
[5]	Memory Full Mode Selection. Options are: 0 = NORMAL. The board is full whenever all buffers are full; 1 = ONE BUFFER FREE. The board is full whenever Nb-1 buffers are full, where Nb is the overall number of buffers in which the channel memory is divided.
[6]	PLL Reference Clock Source (Desktop/NIM only). Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy Enable (VME only). The LVDS I/Os can be programmed to accept a Busy signal as input, or to propagate it as output. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (Bit[8]=1 in the Front Panel I/O Control register, 0x811C). LVDS I/O New Features register, 0x81A0, should also be configured for nBusy/nVeto.
[9]	LVDS I/O Veto Enable (VME only). The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (Bit[8]=1 in the Front Panel I/O Control register, 0x811C). LVDS I/O New Features register, 0x81A0, should also be configured for nBusy/nVeto.

[10]	Reserved.
[11]	<p>LVDS I/O RunIn Enable Mode (VME only). The LVDS I/Os can be programmed to accept a RunIn signal as input, or to transfer it as output.</p> <p>Options are:</p> <p>0 = starts on RunIn level;</p> <p>1 = starts on RunIn rising edge.</p> <p>NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (Bit[8]=1 in the Front Panel I/O Control register, 0x811C). LVDS I/O New Features register, 0x81A0, should also be configured for nBusy/nVeto.</p>
[31: 12]	Reserved.

## Acquisition Status (0x8104, R, C)

This register monitors a set of conditions related to the acquisition status.

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' is on).
[3]	Event Ready. Indicates if events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	PLL Bypass Mode. This bit drives the front panel 'PLL BYPS' LED. Options are: 0 = PLL bypass mode is not active ('PLL BYPS' is off); 1 = PLL bypass mode is active and the VCX0 frequency directly drives the clock distribution tree ('PLL BYPS' is on). WARNING: before to operate in PLL Bypass Mode, it is recommended to contact CAEN for feasibility.
[7]	PLL Unlock Detect. It is the flag for a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL hasn't had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to the Readout Status register, 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately run mode after RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved

## Software Trigger (0x8108, W, C)

Writing in this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

## Global Trigger Mask (0x810C, R/W, C)

This register sets which signal can contribute to the global trigger generation.

Bit	Description
[7:0]	Bit n corresponds to the trigger request from channel n (n=0,...,7) that participates to the global trigger generation.
[19:8]	Reserved. NOTE: in case of DT, NIM and 8-channel VME Boards, bits[19:4] are reserved.
[23:20]	Majority Coincidence Window. Sets the time window (in units of the trigger clock) for the majority coincidence. Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. For a level m, the trigger fires when at least m+1 of the enabled trigger requests (bits[7:0] or [3:0]) are over-threshold inside the majority coincidence window (bits[23:20]). NOTE: The majority level must be smaller than the number of channels enabled via a bits[7:0] mask (or [3:0]).
[28:27]	Reserved.
[29]	LVDS Trigger (VME boards only). When enabled, the trigger from LVDS I/O participates in the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger. When enabled, the external trigger on TRG-IN participates in the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger participates in the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.



## Front Panel TRG-OUT (GPO) Enable Mask (0x8110, R/W, C)

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Bit	Description
[7:0]	Bit n corresponds to the trigger request from channel n (n=0,...,7) that participates to the TRG-OUT signal.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests (bits [7:0] or [3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are between 0 and 7 for VME boards, while between 0 and 3 for DT, NIM and 8-channel VME boards. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled couples of channels (bits [7:0] or [3:0]).
[28:13]	Reserved.
[29]	LVDS Trigger Enable (VME boards only). If the LVDS I/Os are programmed as outputs, they can participate in the TRG-OUT (GPO) signal generation. They are in logic OR with the other enabled signals (bits[31:30] and bits[7:0], or [3:0]). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30], bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.

## LVDS I/O Data (0x8118, R/W, C)

This register allows to readout the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs (REGISTER mode).

NOTE: this register is supported only by VME boards.

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). If the LVDS I/O new features are enabled (bit[8] of 0x811C) and REGISTER mode is set (through 0x81A0), this register allows to read/write from the corresponding nth LVDS I/O according to its configuration. A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input.
[31:16]	Reserved.

## Front Panel I/O Control (0x811C, R/W, C)

This register manages the front panel I/O connectors.

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	LVDS I/O Enable (VME boards only). Enables the 16-pin LVDS I/O front panel connector. Options are: 0 = enabled; 1 = high impedance. NOTE: this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards and LVDS I/O old features only). This configuration must be enabled through bit[8] set to 0. Options are: 00 = general purpose I/O; 01 = programmed I/O; 10 = pattern mode: LVDS signals are input and their value is written into the header PATTERN field; 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.
[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through LVDS I/O New Features register (0x81A0). Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.

[9]	<p>LVDS I/Os Pattern Latch Mode (VME boards only).  Options are:  0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays;  1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives.  NOTE: this bit is reserved in case of DT and NIM boards.</p>
[10]	<p>TRG-IN Signal Edge Disable.  Options are:  0 = the trigger logic is active at the edge of the TRG-IN signal;  1 = the trigger logic is active for the whole duration of the TRG-IN signal.</p>
[11]	<p>TRG-IN to Mezzanines (channels).  Options are:  0 = Standard operating mode: the TRG-IN signal is processed by the motherboard and sent to mezzanine as global trigger;  1 = TRG-IN is directly sent to the mezzanines as global trigger.  This can be useful when the TRG-IN is used to veto the acquisition in conjunction with bit[10] of this register.</p>
[13:12]	Reserved.
[14]	<p>Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1.  Options are:  0 = Force TRG-OUT (GPO) to 0;  1 = Force TRG-OUT (GPO) to 1.</p>
[15]	<p>TRG-OUT (GPO) Mode. Options are:  0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]);  1 = TRG-OUT (GPO) is a test logic level set via bit[14].</p>
[17:16]	<p>TRG-OUT (GPO) Mode Selection.  Options are:  00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to the Front Panel TRG-OUT Enable Mask register, 0x8110;  01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18];  10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe);  11 = S-IN (GPI) propagation.</p>
[19:18]	<p>Motherboard Virtual Probe Selection (to be propagated on TRG-OUT/GPO).  Options are:  00 = RUN: the signal is active when the acquisition is running. This option can be used with VME boards to synchronize the start/stop of the acquisition through the TRG-OUT-&gt;TR-IN or TRG-OUT-&gt;S-IN daisy chain;  01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards;  10 = CLK Phase;  11 = BUSY_UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].</p>
[31:21]	Reserved

[22: 21]	<p>Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format.</p> <p>Options are:</p> <p>00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default);</p> <p>01 = EVENT TRIGGER SOURCE: 16-bit PATTERN indicates the trigger source causing the event acquisition;</p> <p>10 = EXTENDED TRIGGER TIME TAG: enables the Trigger Time Tag information over 48 bits. The 16 most significant bits are given by the 16-bit PATTERN field, while the remaining 32 ones are given by the TRIGGER TIME TAG information in the header of the event format (roll-over bit is not managed).</p> <p>11 = NOT USED: if configured, it acts like 00 setting.</p> <p>NOTE: Refer to the Event Structure section of the digitizer User Manual for a complete information.</p>
[31: 23]	Reserved.

## Channel Enable Mask (0x8120, R/W, C)

This register enables/disables selected channels to participate in the event readout. If disabled, the samples of the relevant channel are lost.

WARNING: this register must not be modified while the acquisition is running.

Bit	Description
[7: 0]	Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled.
[31: 8]	Reserved

## ROC FPGA Firmware Revision (0x8124, R, C)

This register contains information on the motherboard firmware revision (ROC FPGA) in the format X.Y, and the revision date in the format Y/M/DD.

Note that nibble code for the year makes this information to roll over each 16 years.

EXAMPLE 1: revision 3.8 of 12 June 2007 is: 0x76120308.

EXAMPLE 2: revision 4.9 of 7 March 2016 is: 0x03070409.

Bit	Description
[7: 0]	Firmware Minor Revision Number (Y).
[15: 8]	Firmware Major Revision Number (X).
[31: 16]	Revision Date.

## Set Monitor DAC (0x8138, R/W, C)

When the Voltage Level Mode is enabled (through 0x8144), this register sets the DAC value to be provided on the front panel MON/Sigma output LEMO connector: 1 LSB = 0.244 mV, terminated on 50 Ohm.

NOTE: this register is supported only by VME boards.

Bit	Description
[11: 0]	DAC Voltage Setting (VME boards only). The corresponding output value is multiplied by 0.244 mV.
[31: 12]	Reserved.

## Software Clock Sync (0x813C, W, C)

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.

A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.

EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

NOTE: this register is supported by VME boards only.

NOTE: the command must be issued starting from the first to the last board in the clock chain.

NOTE: if a Sync command is intentionally issued, the user must consider that a new channels calibration procedure is needed for a correct board operating (see 0x809C).

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

## Board Info (0x8140, R, C)

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Bit	Description
[7:0]	Digitizer Family Code: 0x0: 724 digitizer family; 0xD: 781 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 1: each channel is equipped with 512 kS acquisition memory; 8: each channel is equipped with 4 MS acquisition memory. For x780 and x781 this is always 1.
[23:16]	Equipped Channels Number. Options are: 0x10 = 16 channels (VME Boards) 0x08 = 8 channels (DT, NIM and 8-channel VME boards). NOTE: if this number is lower than the physical channels number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

## Monitor DAC Mode (0x8144, R/W, C)

This register sets the output DAC mode of the MON/Sigma front panel LEMO connector.

NOTE: this register is supported by VME boards only.

Bit	Description
[2:0]	Monitor DAC Mode (VME boards only). Options are: 000 = Trigger Majority mode; 001 = Test mode; 010 = reserved; 011 = Buffer Occupancy mode; 100 = Voltage Level mode; Others = reserved. Please, refer to the digitizer User Manual for a detailed description.
[31:3]	Reserved.

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## Event Size (0x814C, R, C)

This register contains the current available event in 32-bit words. The value is updated after a complete readout of each event.

Bit	Description
[31: 0]	Event Si ze (32-bi t words).

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## Time Bomb Downcounter (0x8158, R, C)

This is a down counter value. If the value is constant, the firmware license is enabled and the current firmware can be used without any time limitation. If the value decreases with time, the firmware will stop working (no possibility to enter RUN mode) after 30 minutes after module power-on. If the value is 0, the time bomb has expired, and module is not allowed to enter in RUN mode without power cycling the module.

Bit	Description
[31: 0]	Down counter value. If this value is constant the DPP firmware is li censed

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## Memory Buffer Almost Full Level (0x816C, R/W, C)

This register allows to set the level for the Almost Full generation. The written value (ALMOST FULL LEVEL) represents the number of buffers that must be full of data before to assert the BUSY signal. This register takes part in the BUSY propagation among multiple boards. NOTE: if this register is set to 0, the ALMOST FULL is a FULL.

For the Almost Full description, please refer to the Acquisition Synchronization section of the digitizer User Manual.

Bit	Description
[10: 0]	ALMOST FULL LEVEL.
[31: 11]	Reserved.

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## Run/Start/Stop Delay (0x8170, R/W, C)

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles (8 ns for 730 and 725 families) between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Bit	Description
[31: 0]	RUN/START/STOP Del ay (expressed i n t r i g g e r c l o c k c y c l e s, i . e. 10 ns).

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## Board Failure Status (0x8178, R, C)

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.

NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Bit	Description
[3:0]	Internal Communication Timeout. Options are: 0000 = no error; Others = Timeout Error occurred.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved

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## Disable External Trigger (0x817C, R/W, C)

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Bit	Description
[0]	External Trigger on TRG-IN connector can be disabled through this bit. Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

## Trigger Validation Mask (0x8180+(4n) , R/W, I)

Sets the trigger validation logic

Bit	Description
[7: 0]	Bit n corresponds to the trigger request from channel n which participates to the generation of the trigger validation signal.
[9: 8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12: 10]	Sets the majority level. For a level m the majority fires when at least m+1 trigger requests are high.
[27: 13]	Reserved
[28]	LVDS I/O Global Trigger: when enabled (VME form factor only) the global trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[29]	LVDS I/O Individual Trigger: when enabled (VME form factor only) the individual trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.



## Front Panel LVDS I/O New Features (0x81A0, R/W, C)

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).

Options are:

- 1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
- 2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the channel trigger request;
- 3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In in case of input LVDS setting), or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun );
- 4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting).

Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.

NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.

NOTE: this register supported by VME boards only.

Bit	Description
[3: 0]	LVDS I /O pi ns[3: 0] Confi gurati on.
[7: 4]	LVDS I /O pi ns[7: 4] Confi gurati on.
[11: 8]	LVDS I /O pi ns[11: 8] Confi gurati on
[15: 12]	LVDS I /O pi ns[15: 12] Confi gurati on.
[31: 16]	Reserved.

## Readout Control (0xEF00, R/W, C)

This register is mainly intended for VME boards, anyway some of the bits are applicable also for DT and NIM boards.

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,...,7 = sets the VME interrupt level. NOTE: these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). NOTE: this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by the Relocation Address register, 0xEF0C). NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). NOTE: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFFC interval. NOTE: in Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or the bits[31:28] of Relocation Address register (0xEF10). NOTE: this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

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## Readout Status (0xEF04, R, C)

This register contains information related to the readout.

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Output Buffer Status. Indicates if the Output Buffer is in Full condition. Options are: 0 = the Output Buffer is not FULL; 1 = the Output Buffer is FULL.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after a Readout Status register readout (0xEF04).
[31: 3]	Reserved.

---

## Board ID (0xEF08, R/W, C)

The meaning of this register depends on which VME crate it is inserted in.

In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

NOTE: this register is supported by VME boards only.

Bit	Description
[4: 0]	GEO Address (VME boards only).
[31: 5]	Reserved.

---

## MCST Base Address and Control (0xEFOC, R/W, C)

This register configures the board for the VME Multicast Cycles.

NOTE: this register is supported by VME boards only.

Bit	Description
[7: 0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9: 8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31: 10]	Reserved

---

## Relocation Address (0xEF10, R/W, C)

If address relocation is enabled through register 0xEF00, this register sets the VME Base Address of the module.

NOTE: this register is supported by VME boards only.

Bit	Description
[15: 0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of register 0xEF00, this register sets the VME Base Address of the module.
[31: 16]	Reserved.

---

## Interrupt Status/ID (0xEF14, R/W, C)

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

NOTE: this register is supported by VME boards only.

Bit	Description
[31: 0]	STATUS/ID (VME boards only).

---

## Interrupt Event Number (0xEF18, R/W, C)

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Bit	Description
[9: 0]	INTERRUPT EVENT NUMBER.
[31: 10]	Reserved.

---

## Aggregate Number per BLT (0xEF1C, R/W, C)

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Bit	Description
[7: 0]	Number of complete aggregates to be transferred for each block transfer (BLT).

---

## Scratch (0xEF20, R/W, C)

This register can be used to write/read words for test purposes.

Bit	Description
[31: 0]	SCRATCH.

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## Software Reset (0xEF24, W, C)

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

NOTE: a global reset of the module is performed at power-on, which clears the data off the Output Buffer, the event counter and performs a FPGAs global reset restoring them to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

---

## Software Clear (0xEF28, W, C)

All the digitizer internal memories are cleared:

- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command doesn't change the registers actual value, except for resetting the following registers:

- Event Stored;
- Event Size;
- Channel n Buffer Occupancy.

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

---

## Configuration Reload (0xEF34, W, C)

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

---

## Configuration ROM Checksum (0xF000, R, C)

This register contains information on 8-bit checksum of Configuration ROM space.

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

---

## Configuration ROM Checksum Length BYTE 2 (0xF004, R, C)

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

---

## Configuration ROM Checksum Length BYTE 1 (0xF008, R, C)

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Bit	Description
[7: 0]	Checksum Length: bi ts[15: 8].
[31: 8]	Reserved.

---

## Configuration ROM Checksum Length BYTE 0 (0xF00C, R, C)

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Bit	Description
[7: 0]	Checksum Length: bi ts[7: 0].
[31: 8]	Reserved.

---

## Configuration ROM Constant BYTE 2 (0xF010, R, C)

This register contains the third byte of the 3-byte constant.

Bit	Description
[7: 0]	Constant: bi ts[23: 16] = 0x83.
[31: 8]	Reserved.

---

## Configuration ROM Constant BYTE 1 (0xF014, R, C)

This register contains the second byte of the 3-byte constant.

Bit	Description
[7: 0]	Constant: bi ts[15: 8] = 0x84.
[31: 8]	Reserved

---

## Configuration ROM Constant BYTE 0 (0xF018, R, C)

This register contains the first byte of the 3-byte constant.

Bit	Description
[7: 0]	Constant: bi ts[7: 0] = 0x01.
[31: 8]	Reserved.

---

## Configuration ROM C Code (0xF01C, R, C)

This register contains the ASCII C character code (identifies this as CR space).

Bit	Description
[7: 0]	ASCII 'C' Character Code.
[31: 8]	Reserved.

---

## Configuration ROM R Code (0xF020, R, C)

This register contains the ASCII R character code (identifies this as CR space).

Bit	Description
[7: 0]	ASCII 'R' Character Code.
[31: 8]	Reserved.

---

## Configuration ROM IEEE OUI BYTE 2 (0xF024, R, C)

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Bit	Description
[7: 0]	IEEE OUI: bits[23: 16].
[31: 8]	Reserved.

---

## Configuration ROM IEEE OUI BYTE 1 (0xF028, R, C)

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Bit	Description
[7: 0]	IEEE OUI: bits[15: 8].
[31: 8]	Reserved.

---

## Configuration ROM IEEE OUI BYTE 0 (0xF02C, R, C)

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Bit	Description
[7: 0]	IEEE OUI: bits[7: 0].
[31: 8]	Reserved.

---

## Configuration ROM Board Version (0xF030, R, C)

This register contains the board version information.

Bit	Description
[7:0]	Board Version Code. Options for 724 VME form factor are: V1724, VX1724: 0x11 V1724B, VX1724B: 0x40 V1724C, VX1724C: 0x12 V1724D, VX1724D: 0x41 V1724E, VX1724E: 0x42 V1724F, VX1724F: 0x43 V1724G: 0x44. Options for 724 Desktop/NIM form factor are: DT5724/N6724: 0x11 DT5724A/N6724A: 0x13 DT5724D: 0x41 DT5724E: 0x42. Options for 781 digitizer family are: DT5781/N6781: 0xE0; DT5781A/N6781A: 0xE1.
[31:8]	Reserved.

---

## Configuration ROM Board Form Factor (0xF034, R, C)

This register contains the information of the board form factor.

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

---

## Configuration ROM Board ID BYTE 1 (0xF038, R, C)

This register contains the MSB of the 2-byte board identifier.

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

---

## Configuration ROM Board ID BYTE 0 (0xF03C, R, C)

This register contains the LSB information of the 2-byte board identifier.

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.



---

## Configuration ROM PCB Revision BYTE 3 (0xF040, R, C)

This register contains information on the fourth byte of the 4-byte hardware revision.

Bit	Description
[7: 0]	PCB Revi si on: bi ts[31: 24].
[31: 8]	Reserved.

---

## Configuration ROM PCB Revision BYTE 2 (0xF044, R, C)

This register contains information on the third byte of the 4-byte hardware revision.

Bit	Description
[7: 0]	PCB Revi si on: bi ts[23: 16].
[31: 8]	Reserved.

---

## Configuration ROM PCB Revision BYTE 1 (0xF048, R, C)

This register contains information on the second byte of the 4-byte hardware revision.

Bit	Description
[7: 0]	PCB Revi si on: bi ts[15: 8].
[31: 8]	Reserved.

---

## Configuration ROM PCB Revision BYTE 0 (0xF04C, R, C)

This register contains information on the first byte of the 4-byte hardware revision.

Bit	Description
[7: 0]	PCB Revi si on: bi ts[7: 0].
[31: 8]	Reserved.

---

## Configuration ROM FLASH Type (0xF050, R, C)

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Bit	Description
[7: 0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH. NOTE: for 730 and 725 families, this byte must be 0x01.
[31: 8]	Reserved.

---

## Configuration ROM Board Serial Number BYTE 1 (0xF080, R, C)

This register contains information on the MSB of the board serial number.

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

---

## Configuration ROM Board Serial Number BYTE 0 (0xF084, R, C)

This register contains information on the LSB of the board serial number.

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

---

## Configuration ROM VCXO Type (0xF088, R, C)

This register contains information on which type of VCXO is present on-board.

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: 0 = AD9520-3.