

User Manual UM2792

## V1730/VX1730 & V1725/VX1725

16/8-channel 14-bit 500/250 MS/s Waveform Digitizer

Rev. 2 - 10 June 2016

## Purpose of this Manual

This document contains the full hardware description of the V1730 and V1725 CAEN digitizers and their principle of operating as Waveform Digitizer (basing on the hereafter called *default firmware*).

Firmware version of reference: 4.8\_0.5

For any reference to registers in this user manual, please refer to document [RD3] at the digitizer web page.

## Change Document Record

Date	Revision	Changes
03 February 2014	00	Initial release
15 December 2014	01	Added new § 6 on temperature protection. Introduced temperature monitoring safety notices. Updated the § Trigger Management.
10 June 2016	02	Fully reviewed to the new V1725 digitizer (250 MS/s). Updated § 3, § 5, § 7, § Clock Distribution, § PLL Mode, § Output Clock, § Channel Calibration, § Multi-Event Memory Organization, § Event Structure, § Acquisition Synchronization, § Trigger Distribution, § Mode 1: TRIGGER, § Buffer Occupancy Mode ( <i>Monitor Mode</i> = 011), § DPP-PSD Control Software, § 12. Added § CAENScope, § MC2Analyzer (MC2A).

## Symbols, Abbreviated Terms and Notation

GUI	Graphical User Interface
DPP	Digital Pulse Processing
OS	Operating System
PLL	Phase-Locked Loop
PSD	Pulse Shape Discrimination
TTT	Trigger Time Tag

## Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide

[RD2] AN2086 – Synchronization of a multi-board acquisition system with CAEN digitizers

[RD3] UM5118 – UM5118 – 730-725 Families Default Firmware Registers

[RD4] UM1934 - CAENComm User & Reference Manual

[RD5] UM1935 - CAENDigitizer User & Reference Manual

[RD6] UM2091 - CAEN WaveDump User Manual

[RD7] GD2483 - WaveDump QuickStart Guide

[RD8] UM2092 - CAENSCOPE User Manual

[RD9] UM2580 - Digital Pulse Shape Discriminator (DPP-PSD) User Manual

[RD10] UM3182 - DPP-PHA and MC<sup>2</sup>Analyzer User Manual

[RD11] GD2728 – How to make Coincidences with CAEN Digitizers

All documents can be downloaded at: <http://www.caen.it/csite/LibrarySearch.jsp>

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# Safety Notices

**CAUTION:** this product needs proper cooling.



**USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!**

CAEN HEARTLY RECOMMENDS TO MONITOR THE TEMPERATURE OF THE ADC CHIPS DURING THE BOARD OPERATION BY READING AT REGISTER ADDRESS 0x1nA8 (SEE **[RD3]** FOR DETAILS)



**V1730/VX1730 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!**

**CAUTION:** this product needs proper handling.



**ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!**

# 1 Introduction

The Mod. V1730 is 1-unit wide VME 6U module housing a 16-channel 14-bit 500 MS/s FLASH ADC Waveform Digitizer with software selectable  $2 V_{pp}$  or  $0.5 V_{pp}$  input dynamic range on single ended MCX coaxial connectors. The DC offset is adjustable in the  $\pm 1 V$  ( $@2V_{pp}$ ) or  $\pm 0.25$  ( $@0.5V_{pp}$ ) range via a 16-bit DAC on each channel (see § **Analog Input Stage**). A 8-channel version is available by ordering option (see **Tab. 1.1**).

Operationally, the mod. V1725 differs from the V1730 for operating at 250 MS/s sampling frequency.

The ADC resolution and the sampling frequency make these digitizers well suited for mid-fast signal detection systems (e.g. liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers).

Each channel has a SRAM Multi-Event Buffer divisible into  $1 \div 1024$  buffers of programmable size. Two sizes of the channel digital memory are available by ordering options (see **Tab. 1.1**).

V1730 and V1725 digitizers are provided with FPGAs that can run special DPP firmware for Physics Applications (see § **12**).

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, each channel is able to generate a self-trigger when the input signal goes under/over a programmable threshold. For each couple of adjacent channels, the relevant self-triggers are then processed to provide out a single trigger request. In the DPP firmware, the trigger requests can be used at channel level for the event acquisition (independent triggering), while in the default firmware they can be processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. The trigger from one board can be propagated to the other boards through the front panel TRG OUT connector.

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer.

V1730 and V1725 feature front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all V1730 or all V1725 can be synchronized to a common clock source and ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across the multi-board system. CLK-IN / CLK-OUT connectors allow for a Daisy-chained clock distribution.

16 general purpose LVDS I/Os also FPGA-controlled can be programmed for Busy, Data Ready, Memory Full or Individual Trig-Out management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (See § **Front Panel LVDS I/Os**).

An analog output (MON/ $\Sigma$ ) from internal 12-bit 100-MHz DAC controlled by the FPGA allows to provide out four types of information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see § **Analog Monitor**).

V1730 and V1725 are equipped with a VME64 interface (VM64X in case of VX1730 and VX1725) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME, 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface (CAEN proprietary CONET protocol) supporting transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a A3818 (4-link version).



Board Models		Description	Product Code
V1730	16 ch. 14bit 500 MS/s Digitizer: 640kS/ch, CE30, SE		WV1730XAAAAA
V1730B	16 ch. 14bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE		WV1730BXAAAA
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE		WV1730CXAAAA
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE		WV1730DXAAAA
VX1730	16 ch. 14bit 500 MS/s Digitizer: 640kS/ch, CE30, SE		WVX1730XAAAA
VX1730B	16 ch. 14bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE		WVX1730BXAAA
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE		WVX1730CXAAA
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE		WVX1730DXAAA
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE		WV1725XAAAAA
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE		WV1725BXAAAA
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE		WV1725CXAAAA
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE		WV1725DXAAAA
VX1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE		WVX1725XAAAA
VX1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MSch, CE30, SE		WVX1725BXAAA
VX1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/c, CE30, SE		WVX1725CXAAA
VX1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE		WVX1725DXAAA
DPP Firmware (*)		Description	Product Code
DPP-PSD (730 family)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x730): Single-license		WFWDPPTNGAA30
DPP-PSD (725 family)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x725): Single-license		WFWDPPTNGAA25
DPP-PHA (730 family)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x730): Single-license		WFWDPPTFAA30
DPP-PHA (725 family)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis(x725): Single-license		WFWDPPTFAA25
Related Products		Description	Product Code
A2818	A2818 – PCI Optical Link (Rhos compliant)		WA2818XAAAAA
A3818A	A3818A – PCIe 1 Optical Link		WA3818AXAAAA
A3818B	A3818B – PCIe 2 Optical Link		WA3818BXAAAA
A3818C	A3818C – PCIe 4 Optical Link		WA3818CXAAAA
V1718	V1718 - VME-USB 2.0 Bridge		WV1718XAAAAA
V1718LC	V1718LC - VME-USB 2.0 Bridge (Rohs Compliant)		WV1718LCXAAA
VX1718	VX1718 - VME-USB 2.0 Bridge		WVX1718XAAAA
VX1718LC	VX1718LC - VME-USB 2.0 Bridge (Rohs Compliant)		WV1718LCXAAA
V2718	V2718 - VME-PCI Bridge		WV2718XAAAAA
V2718LC	V2718LC - VME-PCI Bridge (Rohs compliant)		WV2718LCXAAA
VX2718	VX2718 - VME-PCI Bridge		WVX2718XAAAA
VX2718LC	VX2718LC - VME-PCI Bridge		WVX2718LCXAA
V2718LC KIT	V2718KITLC - VME-PCI Bridge (V2718)+PCI Optical Link (A2818)+Optical Fibre 5m duplex (AY2705) (Rohs)		WK2718LCXAAA
V2718 KIT	V2718KIT - VME-PCI Bridge (V2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)		WK2718XAAAAA
V2718 KIT-B	V2718KITB - VME-PCI Bridge (V2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)		WK2718XBAAAA
VX2718LC KIT	VX2718KITLC - VME-PCI Bridge (VX2718)+PCI Optical Link (A2818)+Optical Fibre 5m duplex (AY2705) (Rohs)		WKX2718LCXAA
VX2718 KIT	VX2718KIT - VME-PCI Bridge (VX2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)		WKX2718XAAAA
VX2718 KIT-B	VX2718KITB - VME-PCI Bridge (VX2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)		WKX2718XBAAA
Accessories		Description	Product Code
A317	Clock Distribution Cable		WA317XAAAAAA
A318	SE to Differential Clock Adapter		WA318XAAAAAA
A654	Single Channel MCX to LEMO Cable Adapter		WA654XAAAAAA
A654 KIT4	4 MCX TO LEMO Cable Adapter		WA654K4AAAAA
A654 KIT8	8 MCX TO LEMO Cable Adapter		WA654K8AAAAA
A659	A659 - Single Channel MCX to BNC Cable Adapter		WA659XAAAAAA
A659 KIT4	4 MCX TO BNC Cable Adapter		WA659K4AAAAA
A659 KIT8	8 MCX TO BNC Cable Adapter		WA659K8AAAAA
AI2730	Optical Fibre 30 m simplex		WAI2730XAAAA
AI2720	Optical Fibre 20 m simplex		WAI2720XAAAA
AI2705	Optical Fibre 5 m simplex		WAI2705XAAAA

AI2703	Optical Fibre 30 cm simplex	WAI2703XAAAA
AY2730	Optical Fibre 30 m duplex	WAY2730XAAAA
AY2720	Optical Fibre 20 m duplex	WAY2720XAAAA
AY2705	Optical Fibre 5 m duplex	WAY2705XAAAA

**Tab. 1.1:** Table of models and related items

(\*) Multi-license packs are also available. Please, refer to the Digitizer web page for the relevant ordering options.

## 2 Block Diagram

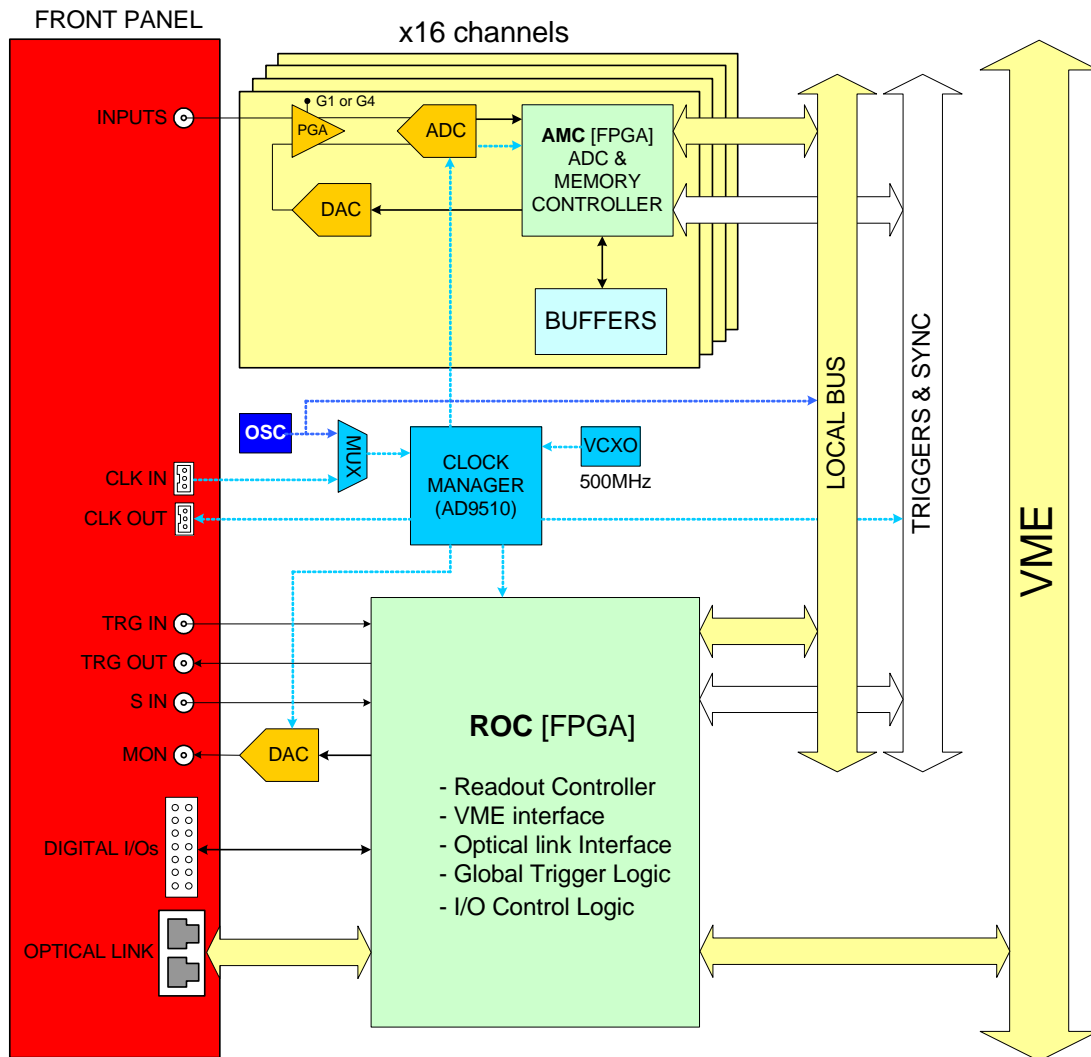


Fig. 2.1: Block Diagram

# 3 Technical Specifications

GENERAL	Form Factor 1-unit wide, 6U VME64 (V1730/V1725) and VME64X (VX1730/VX1725)		
ANALOG INPUT	<b>Channels</b> 16 / 8 channels <sup>(1)</sup> Single ended	<b>Connector</b> MCX	<b>Bandwidth</b> 250 MHz (V1730) 125 MHz (V1725)
	<b>Impedance</b> Z <sub>in</sub> = 50 Ω	<b>Full Scale Range</b> 0.5 or 2 V <sub>pp</sub> (default) SW selectable	<b>Offset</b> Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1 V (@2V <sub>pp</sub> ), ±0.25 V (@0.5V <sub>pp</sub> )
	<sup>(1)</sup> “size1 / size2” denotes different model versions		
DIGITAL CONVERSION	<b>Resolution</b> 14 bits	<b>Sampling Rate</b> 500 MS/s Simultaneously on each channel (V1730) 250 MS/s Simultaneously on each channel (V1725)	
ADC CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	<b>CLK-IN (AMP Modu II)</b> AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter<100ppm requested	<b>CLK-OUT (AMP Modu II)</b> DC coupled differential LVDS clock output locked at ADC sampling clock	<b>S-IN (LEMO)</b> SYNC/START front panel digital input NIM/TTL Z <sub>in</sub> = 50 Ω
	<b>TRG-IN (LEMO)</b> External trigger digital input NIM/TTL; Z <sub>in</sub> = 50 Ω	<b>TRG-OUT (LEMO)</b> Trigger digital output NIM/TTL; R <sub>t</sub> = 50 Ω	
MEMORY	640 kS/ch or 5.12 MS/s Multi-event Buffer divisible into 1 ÷ 1024 buffers Independent read and write access; programmable event size and pre/post-trigger		
TRIGGER	<b>Trigger Source</b> <i>Self-trigger</i> channel over/under-threshold for Common (default firmware) or Individual (DPP firmware only) Trigger generation <i>External-trigger</i> : Common Trigger by TRG-IN or individual by LVDS (DPP firmware only) connector <i>Software-trigger</i> : Common Trigger by software command	<b>Trigger Propagation</b> TRG-OUT programmable digital output  <b>Trigger Time Stamp</b> <i>Default FW</i> : 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension available by firmware <i>DPP-PHA/DPP-PSD FW (V1730)</i> : 31-bit counter, 2 ns resolution, 4 s range; 47-bit extension available by firmware; 10-bit and 2 ps fine time stamp by digital CFD (DPP-PSD FW only); 64-bit extension available by software <i>DPP-PHA/DPP-PSD FW (V1725)</i> : 31-bit counter, 4 ns resolution, 8 s range; 47-bit extension available by firmware; 10-bit and 4 ps fine time stamp by digital CFD (DPP-PSD FW only); 64-bit extension available by software	
	<b>Clock Propagation</b> <i>Daisy chain</i> : through CLK-IN/CLK-OUT connectors <i>One-to-many</i> : clock distribution from an external clock source on CLK-IN connector Clock Cable delay compensation	<b>Acquisition Synchronization</b> Sync, Start/Stop through digital I/O (S-IN or TRG-IN inpu TRG-OUT output)  <b>Trigger Time Stamps Alignment</b> By S-IN input connector	
ADC & MEMORY CONTR.	Altera Cyclone EP4CE30 (one FPGA serves 4 channels).		
COMMUNICATION INTERFACE	<b>Optical Link</b> CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	<b>VME</b> VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)	
ANALOG MONITOR	12-bit / 125MHz DAC FPGA controlled; four operating modes: Test pulses: 1Vpp ramp generator Majority signal: proportional to the nr. Of channels under/over threshold (steps of 125 mV) Memory Occupancy signal: proportional to the Multi Event Buffer Occupancy (1 buffer ~ 1mV) Voltage level: programmable output voltage level		

<b>LVDS I/O</b>	16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker			
<b>DPP FW SUPPORTED</b>	DPP-PSD for the Pulse Shape Discrimination (e.g. Neutron-Gamma discrimination) DPP-PHA for the Pulse Height Analysis			
<b>FIRMWARE UPGRADE</b>	Firmware can be upgraded via VMEbus/Optical Link			
<b>SOFTWARE</b>	General purpose C libraries, configuration tools, readout software (Windows and Linux support)			
<b>POWER CONSUMPTIONS</b>	<b>Mod./Supply Rail</b>	<b>@ +5V</b>	<b>@ +12 V</b>	<b>@ -12V</b>
	<b>V1730</b>	8.2 A	840 mA	<i>not used</i>
	<b>V1730B</b>	10.2 A	840 mA	<i>not used</i>
	<b>V1730C</b>	5 A	400 mA	400 mA
	<b>V1730D</b>	6.5 A	400 mA	400 mA
	<b>V1725</b>	5.2 A	750 mA	<i>not used</i>
	<b>V1725B</b>	<i>t.b.d</i>	<i>t.b.d</i>	<i>t.b.d</i>
	<b>V1725C</b>	<i>t.b.d</i>	<i>t.b.d</i>	<i>t.b.d</i>
	<b>V1725D</b>	<i>t.b.d</i>	<i>t.b.d</i>	<i>t.b.d</i>

**Tab. 3.1:** Specifications table

## 4 Packaging and Compliance

V1725/VX1725 and V1730/VX1730 modules are 1-unit wide, 6U VME64/VME64X boards.

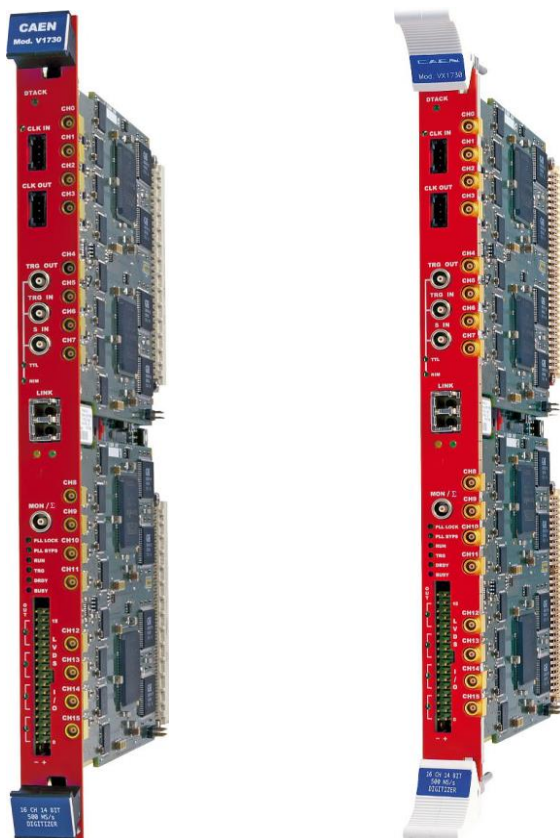


Fig. 4.1: Model view

### 8-Channel Versions

8-channel versions of the V1730/V1725 and VX1730/VX1725 digitizers (see **Tab. 1.1**) differ from 16-channel ones for mounting only the mezzanine managing the analog input channels from 0 to 7. From a functional point of view, what described in this manual applies identically to 8-channels versions.

**CAUTION:** to manage the product, consult the operating instructions provided.



**A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!**

**CAUTION:** this product needs proper cooling.



**USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!**

CAEN HEARTLY RECOMMENDS TO MONITOR THE TEMPERATURE OF THE ADC CHIPS DURING THE BOARD OPERATION BY READING AT REGISTER ADDRESS 0x1nA8 (SEE [RD3] FOR DETAILS)



**V1730/VX1730 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!**

**CAUTION:** this product needs proper handling.



**ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!**

CAEN provides the specific document “Precautions for Handling, Storage and Installation”, available in the documentation tab of the product’s web page, that the user is mandatory to read before to operate with CAEN equipment.

## 5 Power Requirements

The table below resumes the V1730/VX1730/V1725/VX1725 power consumptions per relevant power supply rail.

MODULE	SUPPLY VOLTAGE		
	+5V	+12V	-12V
V1730/VX1730	8.2 A	840 mA	not used
V1730B/VX1730B	10.2 A	840 mA	not used
V1730C/VX1730C	5 A	400 mA	400 mA
V1730D/VX1730D	6.5 A	400 mA	400 mA
V1725/VX1725	5.2 A	750 mA	not used
V1725B/VX1725B	<i>t.b.d.</i>	<i>t.b.d.</i>	<i>t.b.d.</i>
V1725C/VX1725C	<i>t.b.d.</i>	<i>t.b.d.</i>	<i>t.b.d.</i>
V1725D/VX1725D	<i>t.b.d.</i>	<i>t.b.d.</i>	<i>t.b.d.</i>

**Tab. 5.1:** Power requirements table



## 6 Temperature Protection

*TEMPERATURE PROTECTION IS NOT AVAILABLE FOR DEFAULT FIRMWARE RELEASES < 4.5\_0.3 (REFER TO § 12)*

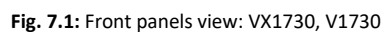
To preserve hardware damages, the V1730 and V1725 implement an automatic turning off of the board channels in event of internal over-temperature. Internal temperature can be monitored by reading at register address 0x1nA8.

The over-temperature limit is fixed at 70°C. As soon as the internal temperature exceeds 70°C, the board enters the temperature protection condition and the firmware automatically performs the following actions:

- turns off all the channel ADCs;
- stops the acquisition, if running (data possibly stored at that moment can be readout in any case).



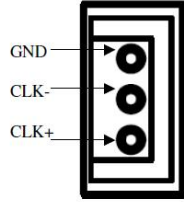
This status is valid as long as the internal temperature remains over 62°C. Starting from 61°C, the user is allowed to turn on the channel ADCs again and restart the acquisition, if necessary.

The temperature protection can be controlled by register addresses 0x8104 and 0x81C0.




V1725 features the same front panel as V1730; so for VX1725 and VX1730.

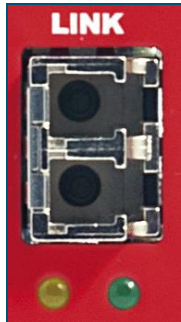
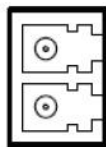
## Front Panel

ANALOG INPUT		
	<b>FUNCTION</b> Input connectors (CH0 to CH15) receiving the input analog signals.	<b>MECHANICAL SPECS</b> Series: MCX connectors. Type: CS 85MCX-50-0-16. Manufacturer: SUHNER Suggested plug: MCX-50-2-16 type. Suggested cable: RG174 type.
	<b>ELECTRICAL SPECS</b> Input dynamics: 2 or 0.5 V <sub>pp</sub> (SW selectable). Input impedance (Z <sub>in</sub> ): 50 Ω.	
CLK IN / CLK OUT		
	<b>FUNCTION</b> Input and output connectors for the external clock.	<b>MECHANICAL SPECS</b> Series: AMPMODU connectors. Type: 3-102203-4 (3-pin). Manufacturer: AMP Inc.
	<b>ELECTRICAL SPECS</b> Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML). CAEN provides single ended-to-differential A318 cable adapter (see <b>Tab. 1.1</b> ) for CLK-IN. Coupling: AC (CLK-IN); DC (CLK-OUT). Z <sub>diff</sub> : 100 Ω.	<b>PINOUT</b> 

**CLK IN LED (GREEN):** indicates the external clock is enabled.

TRG IN / TRG OUT / S IN		
	<b>FUNCTION</b> <ul style="list-style-type: none"> <li>• TRG-OUT: digital output connector to propagate <ul style="list-style-type: none"> <li>– the internal trigger sources;</li> <li>– the channel probes (i.e. signals from the mezzanines);</li> <li>– S-IN signal</li> </ul> </li> </ul> <p>according to register addresses 0x8110 and 0x811C, or</p> <ul style="list-style-type: none"> <li>– the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal</li> </ul> <p>according to register address 0x811C.</p> <ul style="list-style-type: none"> <li>• TRG-IN: digital input connector for the external trigger.</li> <li>• S-IN: SYNC/START/STOP digital input connector configurable as reset of the time stamp (see § <b>Timer Reset</b>) or to start/stop the acquisition (see § <b>Acquisition Run/Stop</b>).</li> </ul>	<b>MECHANICAL SPECS</b> <p>Series: 101 A 004 connectors.</p> <p>Type: DLP 101 A 004-28.</p> <p>Manufacturer: FISCHER.</p> <p><b>Alternatively:</b></p> <p>Type: EPL 00 250 NTN.</p> <p>Manufacturer: LEMO.</p>
	<b>ELECTRICAL SPECS</b> <p>Signal level: NIM or TTL.</p> <p>TRG-IN/S-IN Input impedance (<math>Z_{in}</math>): 50 <math>\Omega</math></p> <p>TRG-OUT requires 50 <math>\Omega</math> termination.</p>	

**TTL (GREEN), NIM (GREEN):** indicate the standard TTL or NIM is set for TRG-OUT, TRG-IN, S-IN.

OPTICAL LINK PORT		
	<b>FUNCTION</b> <p>Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125<math>\mu</math>m cable featuring LC connectors on both sides.</p>	<b>MECHANICAL SPECS</b> <p>Series: SFF Transceivers.</p> <p>Type: FTLF8519F-2KNL (LC connectors).</p> <p>Manufacturer: FINISAR.</p>
	<b>ELECTRICAL SPECS</b> <p>Transfer rate: up to 80 MB/s.</p>	<b>PINOUT</b>  <p>TX (red wrap)</p> <p>RX (black wrap)</p>

**LINK LEDs (GREEN/YELLOW):** right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

## MON / $\Sigma$



### FUNCTION

Analog Monitor output connector with 4 programmable modes (see § **Analog Monitor**):

- Trigger Majority
- Test Pulses
- Memory Occupancy
- Voltage Level

### ELECTRICAL SPECS

12-bit (100 MHz) DAC output, 1V<sub>pp</sub> on R<sub>t</sub>=50 Ω

### MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

### Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO

## DIAGNOSTICS LEDs



**DTACK (GREEN)**: indicates there is a VME read/write access to the board;

**PLL LOCK (GREEN)**: indicates the PLL is locked to the reference clock;

**PLL BYPS (GREEN)**: indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off;

**RUN (GREEN)**: indicates the acquisition is running (data taking). See §

### Acquisition Run/Stop

**TRG (GREEN)**: indicates the trigger is accepted.

**DRDY (GREEN)**: indicates the event/data is present in the Output Buffer.

**BUSY (RED)**: indicates all the buffers are full for at least one channel.

## LVDS I/Os CONNECTOR



### FUNCTION

16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15.

In/Out direction is software controlled.

Different selectable modes (see § **Front Panel**

### LVDS I/Os):

- Register
- Trigger
- nBusy/nVeto
- Legacy

### ELECTRICAL SPECS

Level: differential LVDS

Z<sub>diff</sub>: 100 Ω



### MECHANICAL SPECS

Series : TE - AMPMODU Mod II Series

Type: 5-826634-0 (lead spacing: 2.54mm; row pitch: 2.54mm)

Manufacturer: AMP Inc.

**LVDS I/O LEDs (GREEN)**: Each LED close to a 4-pin group lights on if the pins are set as outputs.

LABELS	
	<p>Two blue labels on each insertion/extraction handle on the VME front panel report:</p> <ul style="list-style-type: none"> <li>– Manufacturer name and board's model</li> <li>– -Brief functional description of the module</li> </ul>
	<p>A little silver label on the bottom of the VME board's front panel reports:</p> <ul style="list-style-type: none"> <li>– 4-digit Serial Number (S/N)</li> </ul>

## Internal Components

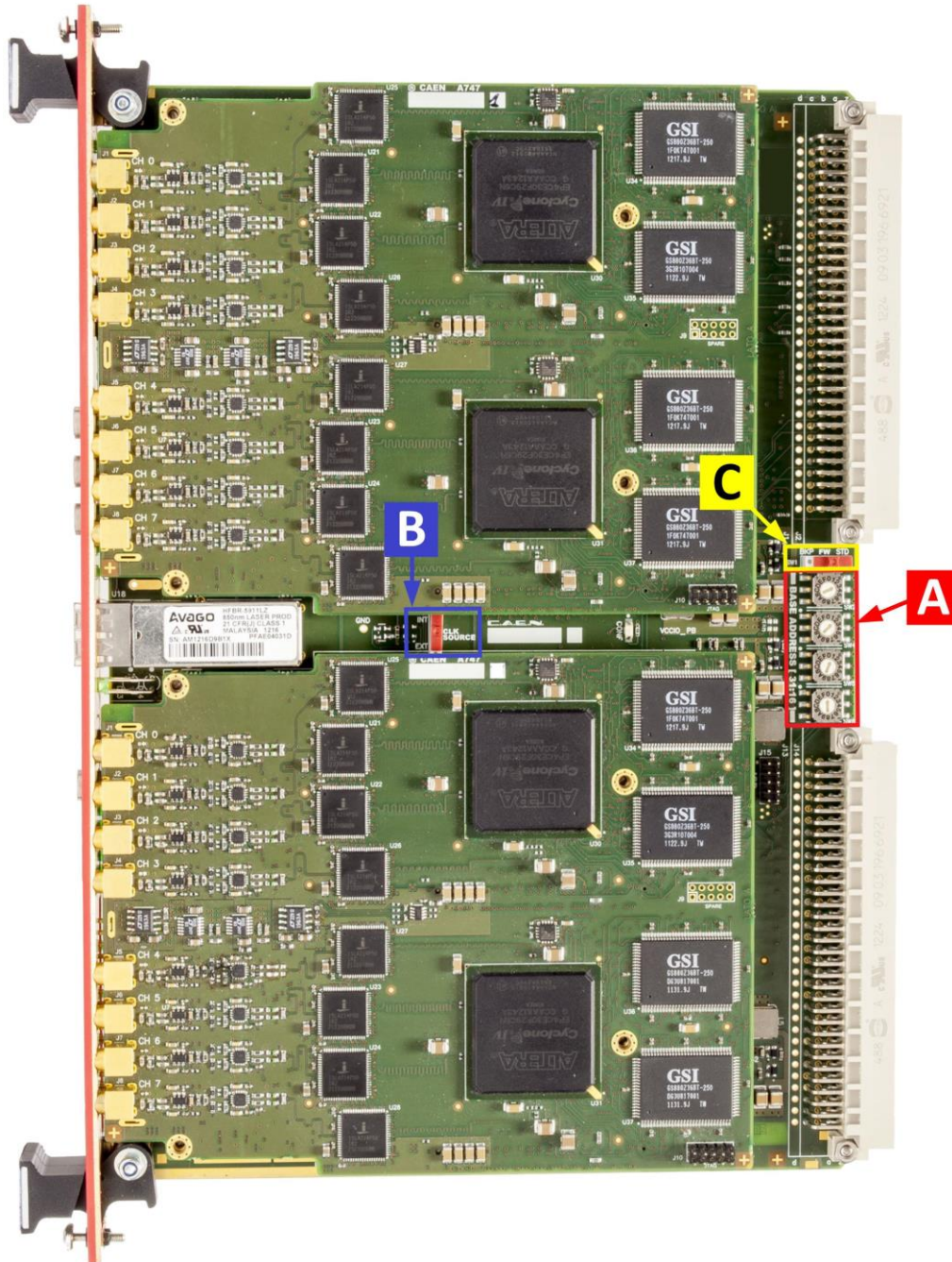


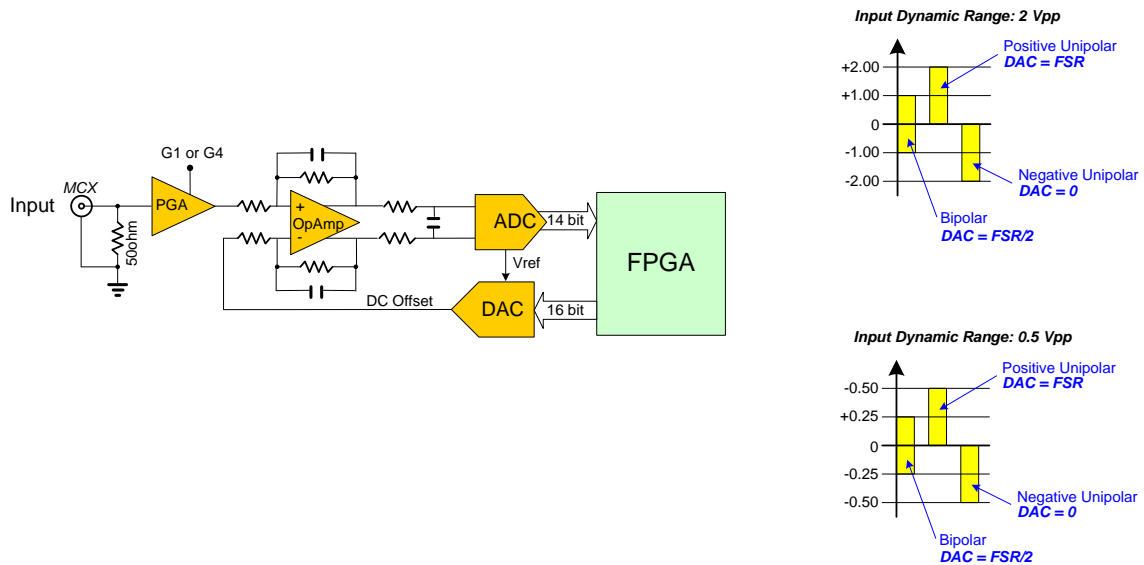
Fig. 7.2: Rotary and dip switches location

<b>A</b>	<b>SW2,4,5,6:</b> "Base Address [31:16]"	<b>Type:</b> Rotary Switches	<b>Function:</b> Set the VME Base Address of the module
<b>B</b>	<b>SW3:</b> "CLOCK SOURCE" INT/EXT	<b>Type:</b> Dip Switch	<b>Function:</b> Selects the clock source (External or Internal)
<b>C</b>	<b>SW1:</b> "FW" BKP/STD	<b>Type:</b> Dip Switch	<b>Function:</b> Selects between the "Standard" (STD) and the "Backup" (BKP) FLASH page as the first to be first read at power-on to load the FW on the FPGAs (default position is STD); see § 12

# 8 Functional Description

## Analog Input Stage

Input dynamics can be  $2 V_{pp}$  (default) or  $0.5 V_{pp}$ , by software selection (basing on the Programmable Gain Amplifier in the scheme of **Fig. 8.1**), on single ended MCX coaxial connectors (see § 6). A 16-bit DAC allows to add a DC offset in order to preserve the full dynamic range also in the extreme case of unipolar positive or negative input signal. The input bandwidth ranges from DC to 250 MHz (@3dB) for V1730, to 125 MHz (@3dB) for V1725, by 2<sup>nd</sup> order linear phase anti-aliasing low-pass filter.



**Fig. 8.1:** Analog Input Diagram

Setting the input range requires a write access at register address 0x1n28, while at register address 0x1n98 it is possible to configure the DC offset level.



## Clock Distribution

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50-MHz clock provided by an on-board oscillator, the latter provides the ADC sampling clock.

OSC-CLK handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in Fig. 8.2).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (fed via front panel signal on CLK-IN) or an internal (via local oscillator) source; in the latter case, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).

V1730 and V1725 use an integrated phase-locked-loop (PLL) and clock distribution device, AD9510. It is used to generate the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0/SAMP-CLK1), as well as the trigger logic synchronization clock (TRG-CLK).

Both clocks can be generated from the internal oscillator (50 MHz) or from external clock input. By default, the board uses the internal clock as PLL reference (REF-CLK).

The external clock can be selected by SW3 on-board switch (see Fig. 7.2). The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100ppm (see § Tab. 3.1).

AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change:

V1730 and V1725 lock to an external 50 MHz clock with default AD9510 configuration; see § PLL Mode.

Refer to the AD9510 datasheet for more details:

[http://www.analog.com/UploadedFiles/Data\\_Sheets/AD9510.pdf](http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf)

(in case the active link above doesn't work, copy and paste it on the internet browser)

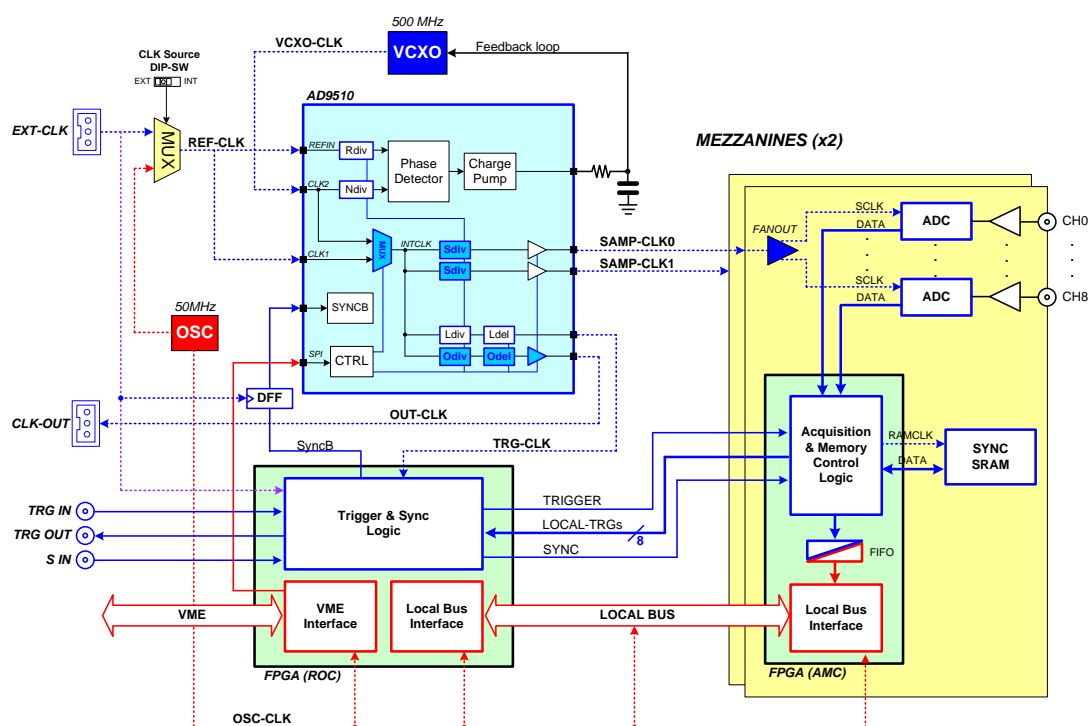


Fig. 8.2: Clock Distribution Diagram

## PLL Mode

The Phase Detector within the AD9510 device allows to couple REF-CLK with a VCXO (500 MHz frequency) providing out the nominal ADCs frequency (500 MHz for V1730 and 250 MHz for V1725); for this purpose, it is necessary that REF-CLK is a submultiple of the VCXO frequency.

As introduced in § **Clock Distribution**, the source of the REF-CLK signal can be external (see **Fig. 8.2**) on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW3 (see **Fig. 7.2**). The following options are allowed:

1. 50 MHz internal clock source – It's the standard operating mode, where the default AD9510 configuration doesn't require to be changed. OSC-CLK = REF-CLK.
2. 50 MHz external clock source – In this case it is not required to reprogram the AD9510 dividers, as the external clock reference is identical to the frequency of the internal oscillator. CLK-IN = OSC-CLK = REF-CLK.
3. External clock source different from 50 MHz – In this case, the user is required to program the AD9510 dividers in order to lock the VCXO to REF-CLK in order to provide out the nominal sampling frequency (500 MHz for V1730 and 250 MHz for V1725). In principle, the allowed external frequencies are submultiples of the VCXO frequency (500 MHz). CLK-IN = REF-CLK.



**Note:** the user who wants to work as in point 3, please contact CAEN indicating the required reference clock frequency to check its feasibility and then receive the PLL programming file. The "Upgrade PLL" function in CAENUpgrader software tool can be used to update the digitizer PLL. See § 10 for the program description and refer to **[RD1]** for documentation.

In order the board to sense the external signal on CLK-IN and use it as new reference (points 2 and 3), the user must set the on-board CLOCK SOURCE switch (SW3) on the EXT position (see **Fig. 7.2**).

## Changing the ADC Frequency

Please, contact CAEN (see § 13) for information on the feasibility to operate the V1730/V1725 with a sampling frequency lower than the nominal.

## Trigger Clock

TRG-CLK signal has a 125-MHz frequency, that is equal to  $\frac{1}{4}$  (V1730) or  $\frac{1}{2}$  (V1725) of SAMP-CLK. In consequence, a 4 samples (V1730) or 2 samples (V1725) "uncertainty" occurs over the acquisition window.

## Output Clock

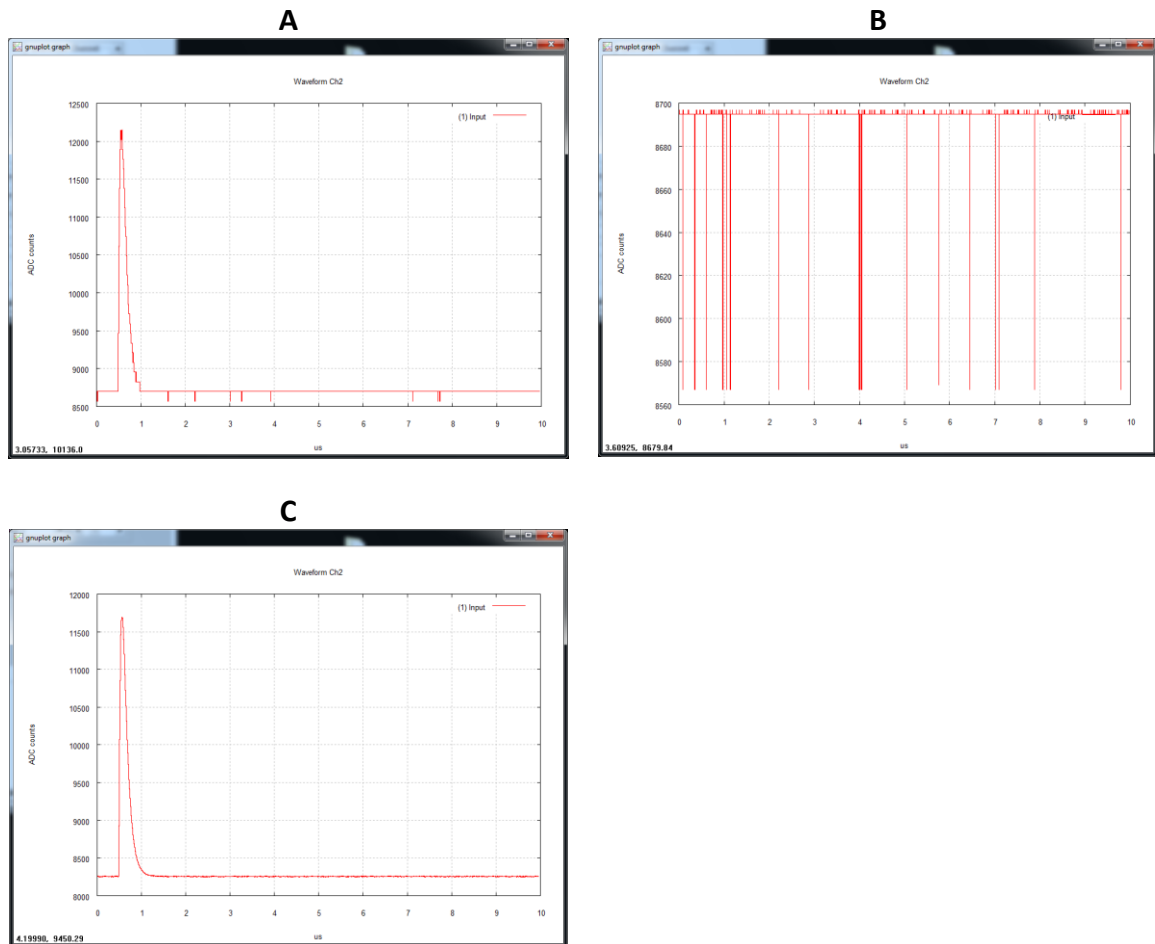
The AD9510 output can be available on the front panel CLK-OUT connector (see § 7). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain.

Please, contact CAEN for information (see § 13).

# Acquisition Modes

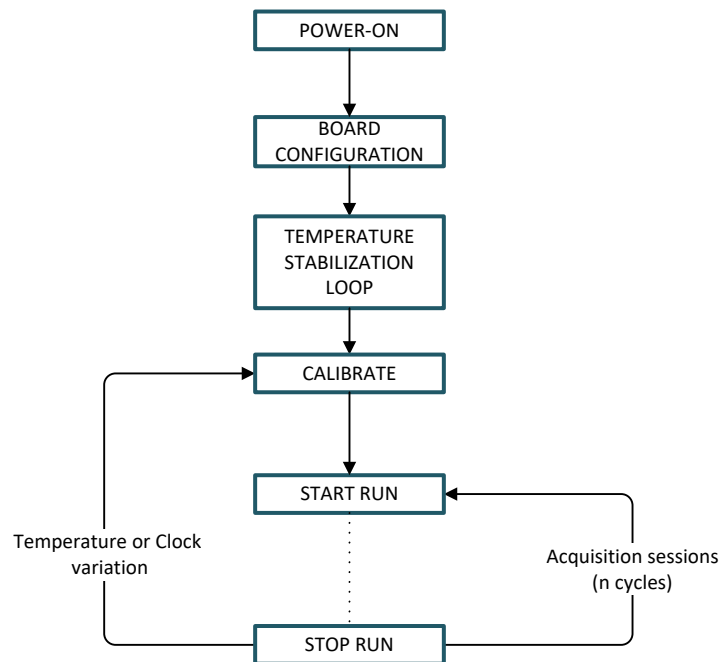
## Channel Calibration

The module performs a self-calibration of the ADCs at its power-on. Anyway, in order to achieve the best performance, the calibration procedure is recommended to be executed by the user, on command, after the ADCs have stabilized their operating temperature. The calibration will not need to be repeated at each run unless the operating temperature changes significantly, or clock settings are modified (e.g. switching from internal to external clock).



**Fig. 8.3:** Typical channel before the calibration (A and B) and after the calibration (C)

The diagram below schematizes the flow for a proper calibration:



- At low level, the ADCs temperature can be read at the register address 0x1nA8, while the calibration must be performed through register address 0x809C. The following steps are required:
  - Write whatever value at register address 0x809C: the self-calibration process will start simultaneously on each channel of the board and the "Calibrating bit" flag of register address 0x1n88 will be set to 0.
  - Poll the "Calibrating bit" flag until it returns to 1.



**Note:** It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at register address 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (indicatively 100 ms) before to start the calibration.



**Note:** At power-on, a Sync command is also issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (write access at register address 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

- At the library level, developers can exploit the CAENDigitizer library (see § 9) dedicated routines which are *ReadTemperature()* function for temperature readings and the *Calibrate()* function which executes the channel calibration steps above described.



**IMPORTANT NOTE:** Starting from CAENDigitizer release 2.6.1, the *Reset()* function has been modified so that it no longer includes the channel calibration routine implemented in the code. This calibration must be performed on command by the dedicated *Calibrate()* function. Please, see the Library user manual for reference ([RD5]).

- At software level, CAEN manages the on command channel calibration in different readout software (please, refer the relevant software User Manual for details).

➤ **WaveDump**

1. Launch WaveDump. This software performs an automatic ADC calibration and displays a message when it is completed (see Fig. 8.4).

```

*****
Wave Dump 3.7.2_20160420
*****
Opening Configuration File WaveDumpConfig.txt
Connected to CAEN Digitizer Model DT5725
ROC FPGA Release is 04.10 - Build 0401
AMC FPGA Release is 00.06 - Build 0401

ADC Calibration successfully executed.

[s] start/stop the acquisition, [q] quit, [SPACE] help

```

Fig. 8.4: Automatic calibration at WaveDump first run

This allows the user to start using the program sure that the digitizer has been calibrated at least once.

**NOTE THAT: If SKIP\_STARTUP\_CALIBRATION parameter is set to YES in WaveDump configuration file, the automatic start-up calibration is not performed and no message is displayed**

2. At any time, the user can check the channel temperatures (with the acquisition not running) by issuing multiple “m” commands from the keyboard.
3. In case of significant variations, issuing a “c” command provokes a manual channel calibration to be executed (see Fig. 8.5).

```

Reading at 4.49 MB/s <Trg Rate: 1137.62 Hz>
Reading at 4.47 MB/s <Trg Rate: 1133.66 Hz>
Acquisition stopped
CH00: 31 C
CH01: 31 C
CH02: 31 C
CH03: 31 C
CH04: 28 C
CH05: 28 C
CH06: 28 C
CH07: 28 C

CH00: 31 C
CH01: 31 C
CH02: 31 C
CH03: 31 C
CH04: 29 C
CH05: 29 C
CH06: 29 C
CH07: 29 C

ADC Calibration successfully executed.

```

Fig. 8.5: Temperature monitoring with manual calibration in WaveDump software

4. A new acquisition can start.

Please, refer to WaveDump User Manual for complete software description ([RD6]).

## ➤ DPP-PSD Control Software

1. Launch DPP-PSD Control Software
2. Connect to the digitizer
3. Before to start the acquisition, go to the “Stats” tab and monitor the channel temperatures displayed in the relevant column until you see they don’t vary significantly
4. Go to the “General” tab and press the “Calibrate” button
5. Start the acquisition

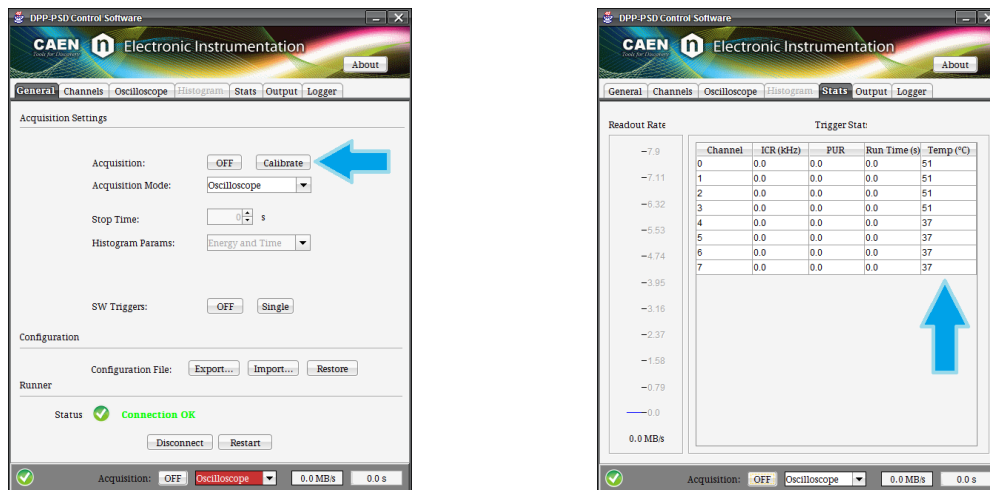


Fig. 8.6: Channel calibration in DPP-PSD Control Software

## ➤ MC<sup>2</sup>Analyzer

1. Launch MC<sup>2</sup>A
2. Connect to the digitizer
3. Before to start the acquisition, monitor the channel temperatures in Tools->ADC calibration
4. Press “Calibrate” button to perform the calibration
5. Start the acquisition

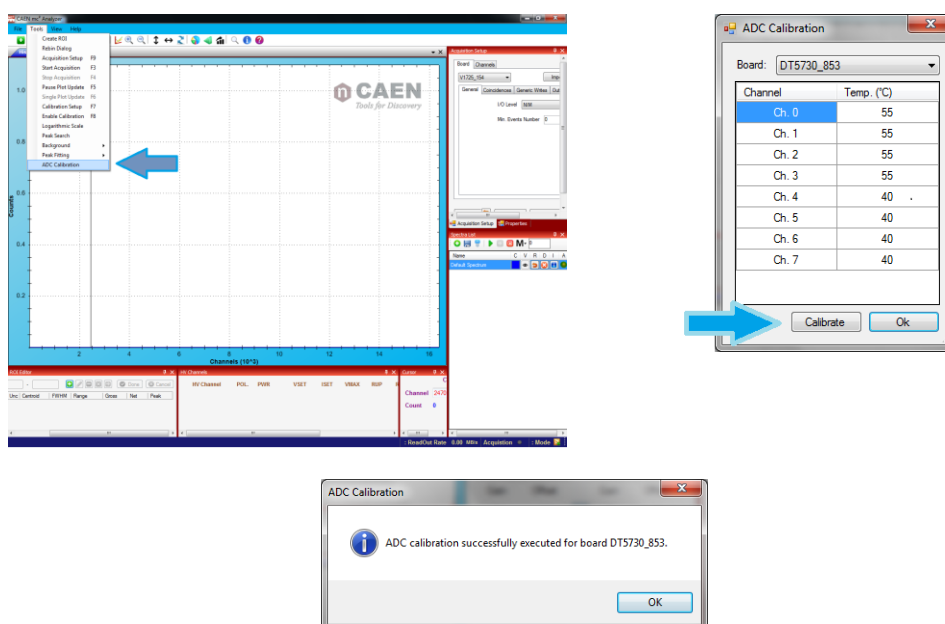


Fig. 8.7: Channel calibration in MC<sup>2</sup>Analyzer software

## Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting at register address 0x8100 and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the S-IN signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see § **Front Panel LVDS I/Os**).

## Acquisition Triggering: Samples & Events

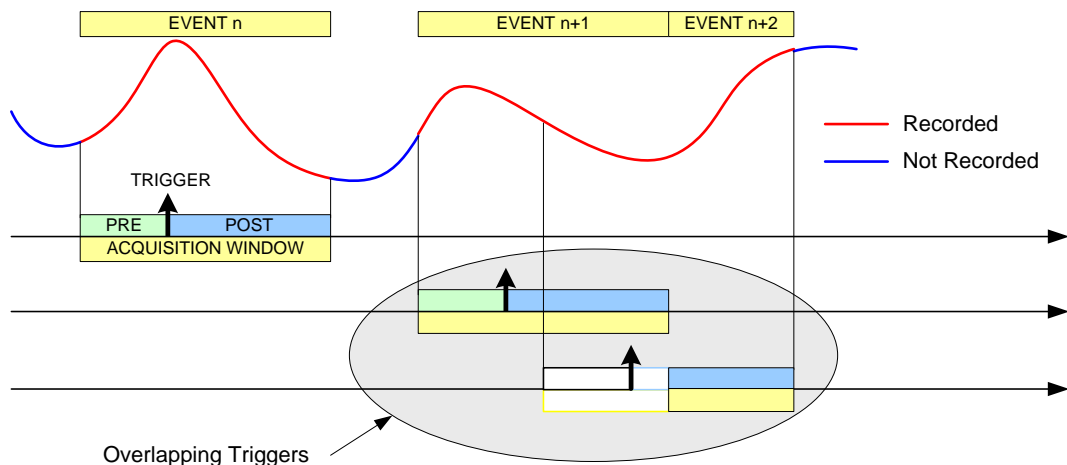
When the acquisition is running, a trigger signal allows to:

- Store the 31-bit counter value of the Trigger Time Tag (TTT).  
The counter (representing a time reference), like so the Trigger Logic Unit (see **Fig. 8.2**) operates at a frequency of 125 MHz (i.e. 8 ns or 4 ADC clock cycles in case of V1730, while 2 ADC clock cycles in case of V1725). Due to the way the acquired data are written into the board internal memory (i.e. in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always “0”.
- Increment the EVENT COUNTER.
- Fill the active buffer with the pre/post-trigger samples, whose number is programmable (Acquisition window width), freezing then the buffer for readout purposes, while acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).

If the board is programmed to accept the overlapped triggers (by programming at register address 0x8000), as the “overlapping” trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case events will not have all the same size (see **Fig. 8.8** below)



**Fig. 8.8:** Trigger overlap

A trigger can be refused for the following causes:

- Acquisition is not active.
- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the *RUN Acquisition* command (see § **Acquisition Run/Stop**) or with respect to a buffer emptying after a *Memory FULL* status (see § **Acquisition Synchronization**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and readout.



## Multi-Event Memory Organization

Each channel of the V1730/V1725 features a SRAM memory to store the acquired events. The memory size for the event storage is 640 kS/ch or 5.12 MS/s, according to the board version (see **Tab. 1.1**), and it can be divided in a programmable number of buffers,  $N_b$  ( $N_b$  from 1 up to 1024), by register address 0x800C, as described in **Tab. 8.1** below.

Register Value	Buffer Number ( $N_b$ )	Size of one Buffer (Samples)	
		SRAM 640 kS/ch <sup>(*)</sup>	SRAM 5.12 MS/ch <sup>(*)</sup>
0x00	1	640k - 10	5.12M - 10
0x01	2	320k - 10	2.56M - 10
0x02	4	160k - 10	1.28M - 10
0x03	8	80k - 10	640k - 10
0x04	16	40k - 10	320k - 10
0x05	32	20k - 10	160k - 10
0x06	64	10k - 10	80k - 10
0x07	128	5k - 10	40k - 10
0x08	256	2560 - 10	20k - 10
0x09	512	1280 - 10	10k - 10
0x0A	1024	640 - 10	5120 - 10

**Tab. 8.1:** Buffer organization

Having 640 kS memory size as reference, this means that each buffer contains  $640k/N_b$  samples (e.g.  $N_b = 1024$  means 640 samples in each buffer).

**(\*)IMPORTANT:** For AMC FPGA firmware release < **0.2**, the Size of one Buffer related to each Buffer Number must be intended as the number of the samples in **Tab. 8.1**. without decreasing by 10 samples.

### Custom Sized Events

In case an event size minor than the buffer size is needed, the user can set the value  $N_{loc}$  at register address 0x8020; the event is so forced to be made by  $10 \cdot N_{loc}$  samples. Setting  $N_{loc} = 0$ , the custom size is disabled. The value of  $N_{loc}$  must be set in order that the relevant number of samples does not exceed the buffer size and it mustn't be modified while the acquisition is running.



**Note:** Even using the custom size setting, the number of buffers and the buffer size are not affected by  $N_{loc}$ , but they are still determined by  $N_b$ .

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The *Record Length* parameter defined in CAEN software (such as WaveDump and CAENScope introduced in § 10) and the *Set/GetRecordLength()* function of the CAENDigitizer library rely on these concepts.

## Event Structure

The event can be readout via VMEbus or Optical Link; data format is 32-bit long word (see **Tab. 8.3**)

An event is structured in:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

**Header** consists in 4 words including the following information:

- **EVENT SIZE (Bit[27:0] of 1<sup>st</sup> header word)** = It is the size of the event (number of 32-bit long words);
- **Board ID (Bit[31:27] of 2<sup>nd</sup> header word)** = It is the GEO address meaningful for VME64X modules;
- **BOARD FAIL FLAG (Bit[26] of 2<sup>nd</sup> header word)** = Implemented from ROC FPGA firmware revision **4.5** on (*reserved* otherwise), this bit is set to “1” in consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition). The user can collect more information about the cause by reading at register address 0x8104 and contact CAEN Support Service if necessary (see § **13**);
- **Bit[24] (2<sup>nd</sup> header word)** = This bit identifies the event format; it is reserved and **must be 0**;
- **Bit[23:8] (2<sup>nd</sup> header word)** = It is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives.



**Note:** Starting from revision **4.6** of the ROC FPGA firmware, these 16 bits can be programmed to provide trigger information according to the setting of the bits[22:21] at register address 0x811C (**Tab. 8.2**).

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	PATTERN INFORMATION (16 bits in the 2 <sup>nd</sup> header word)
00 (default)	PATTERN	Pattern of the 16 LVDS signals.
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 0000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16] = Trigger from LVDS connector Bits[15:8] = Trigger requests from the couple of channels (refer to § <b>Self-Trigger</b> )
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4 <sup>th</sup> header word). <b>Note:</b> in the ETTT option, the overflow bit is not provided.
11	<i>Not used</i>	If configured, it acts like “00” setting.

**Tab. 8.2:** PATTERN configuration table

- **CHANNEL MASK (Bit[7:0] of the 2<sup>nd</sup> and Bit[31:24] of the 3<sup>rd</sup> header word)** = It is the mask of the channels participating in the event. This information must be used by the software to acknowledge which channel the samples are coming from. Channels 7:0 are masked in the 2<sup>nd</sup> header word, while channels 15:8 in the 3<sup>rd</sup> one, as shown in **Tab. 8.3**.
- **EVENT COUNTER (Bit[23:0] of 3<sup>rd</sup> header word)** = This is the trigger counter; it can count either accepted triggers only, or all triggers.

- TRIGGER TIME TAG (Bit[31:0] of 4<sup>th</sup> header word)** = It is the 31-bit Trigger Time Tag information (31-bit counter and 32<sup>nd</sup> bit as roll over flag), which is the trigger time reference. If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2<sup>nd</sup> event word). Note that, in the ETTT case, the roll over flag is no more provided. The trigger time tag is reset either at the start of acquisition, or via front panel signal on S-IN or LVDS I/O connectors, and increments with 125-MHz frequency (every 4 ADC clock cycles in case of V1730 or 2 ADC clock cycles with V1725). The trigger time tag value is read at half this frequency (62.5 MHz). So, the trigger time tag specifications result in 16 ns resolution and 17 s range (i.e.  $8 \text{ ns} \cdot (2^{31}-1)$ ), which can be extended to 625 h (i.e.  $8 \text{ ns} \cdot (2^{48}-1)$ ) by the Extended Trigger Time Tag option.

**Data** are the samples from the enabled channels. Data from masked channels are not read.

### Event Format Example

**Tab. 8.3** shows the event data format of V1730/V1725 when all the 16 channels are enabled. The structure is described in § **Event Structure**.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 0 1 0				EVENT SIZE																											
BOARD ID				BF <sub>RES</sub> 0		PATTERN / TRG OPTIONS																CHANNEL MASK [7:0]									
CHANNEL MASK [15:8]								EVENT COUNTER																							
TRIGGER TIME TAG																															
0 0		SAMPLE [1] – CH[0]												0 0		SAMPLE [0] – CH[0]															
0 0		SAMPLE [3] – CH[0]												0 0		SAMPLE [2] – CH[0]															
...																															
0 0		SAMPLE [N-1] – CH[0]												0 0		SAMPLE [N-2] – CH[0]															
0 0		SAMPLE [1] – CH[1]												0 0		SAMPLE [0] – CH[1]															
0 0		SAMPLE [3] – CH[1]												0 0		SAMPLE [2] – CH[1]															
...																															
0 0		SAMPLE [N-1] – CH[1]												0 0		SAMPLE [N-2] – CH[1]															
...																															
0 0		0 0		SAMPLE [1] – CH[15]												0 0		SAMPLE [0] – CH[15]													
0 0		SAMPLE [3] – CH[15]												0 0		SAMPLE [2] – CH[15]															
...																															
0 0		SAMPLE [N-1] – CH[15]												0 0		SAMPLE [N-2] – CH[15]															

HEADER	
DATA CH0	
DATA CH1	
...	
DATA CH15	

**Tab. 8.3:** Event Format example

## Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number  $N_b$  of circular buffers ( $N_b = [1:1024]$ ; see **Tab. 8.1**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VME or Optical Link. The acquisition can continue without dead-time in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as at least one buffer is read out, the board exits the FULL condition and acquisition restarts.



**Note:** When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting  $\text{bit}[5] = 1$  at register address 0x8100. The board is so programmed to enter the FULL condition when  $N_b - 1$  buffers are written: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is readout and becomes free, the board exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).



**Note:** when  $\text{bit}[5] = 1$ , the minimum number of circular buffers to be programmed is  $N_b = 2$ .

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In this cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level (register address 0x816C) to X, the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is  $N_b$  or  $N_b - 1$ , depending on  $\text{bit}[5]$  at register address 0x8100 as described above.

It is possible to provide the BUSY signal on the digitizer front panel TRG-OUT output ( $\text{bit}[20]$ ,  $\text{bits}[19:18]$  and  $\text{bits}[17:16]$  at register address 0x811C are involved). In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connectors (see § **Front Panel LVDS I/Os**).

## Trigger Management

According to the default firmware operating, all the channels in a board share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (a determined number of samples according to buffer organization and custom size settings, and position with respect to the trigger given by the post-trigger).



**Note:** For the trigger management in the DPP firmware operating, please refer to [RD9] or [RD10].

The generation of a common acquisition trigger is based on different trigger sources (configurable at register address 0x810C):

- Software trigger
- External trigger
- Self-trigger
- LVDS I/O trigger
- Coincidence

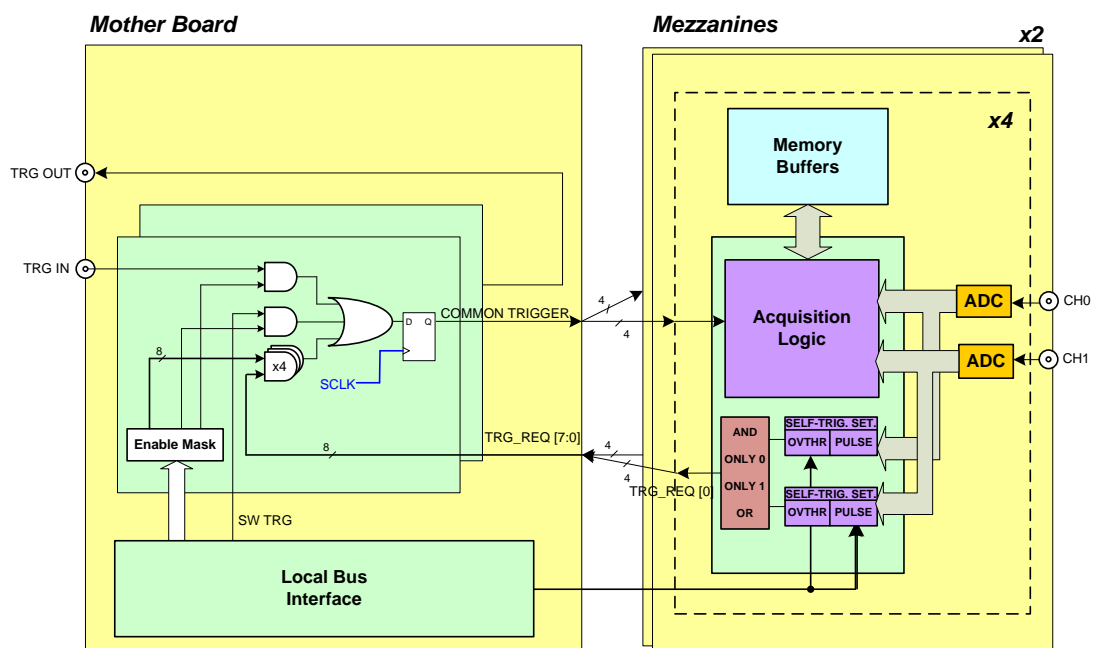


Fig. 8.9: Block Diagram of the trigger management

### Software Trigger

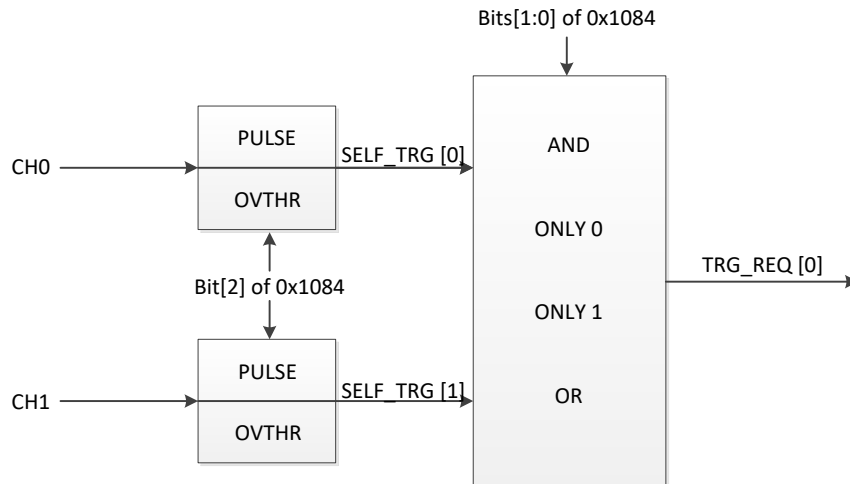
Software triggers are internally produced via a software command (write access at register address 0x8108) through VMEbus or Optical Link.

### External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at register address 0x811C). If the external trigger is not synchronized with the internal clock, a 1-clock period jitter occurs.

## Self-Trigger

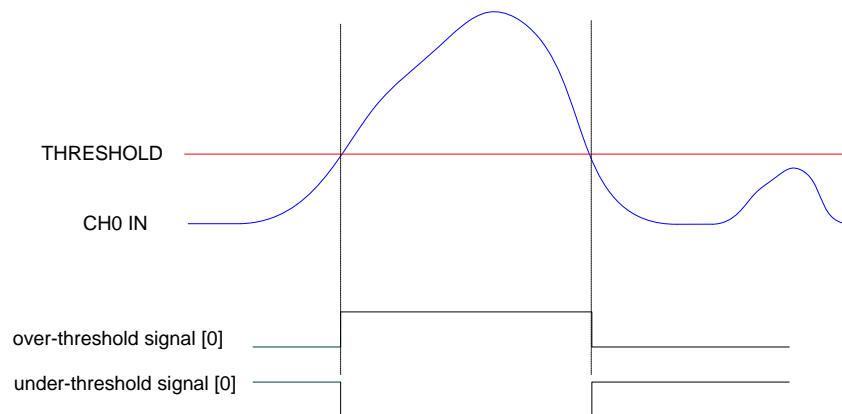
Each channel is able to generate a self-trigger signal when the digitized input pulse exceeds a configurable threshold (register address 0x1n60). The self-triggers of each couple of adjacent channels are then processed to provide out a single trigger request. The trigger requests are propagated to the central trigger logic where they are ORed to produce the board common trigger, which is finally distributed back to all channels causing the event acquisition (see **Fig. 8.9**). **Fig. 8.10** schematizes the self-trigger and trigger request logic having the channel 0 and channel 1 couple as an example.



**Fig. 8.10:** Self Trigger and Trigger Request logic for Ch0 and Ch1 couple. A single trigger request signal is generated.

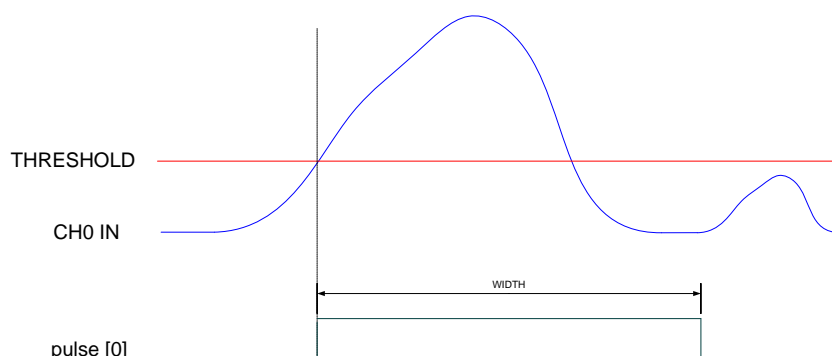
The FPGA, by register address 0x1n84, can be programmed in order the self-trigger to be:

- an *over/under-threshold signal* (see **Fig. 8.11**). This signal can be programmed to be active (i.e. "1") as long as the input pulse is over the threshold or under the threshold (depending on the trigger polarity bit at register address 0x8000).



**Fig. 8.11:** Channel over/under threshold signal

- a pulse of configurable width (see Fig. 8.12). The width parameter can be set at register address 0x1n70.



**Fig. 8.12:** Channel pulse signal

The FPGA, by register address 0x1n84, can be programmed in order the trigger request for a couple of adjacent channels to be the

AND,  
ONLY CH(n),  
ONLY CH(n+1),  
OR

of the relevant self-trigger signals (see Fig. 8.10).

**Default Conditions:** by default, the FPGA is programmed so that the trigger request is the OR of two pulses of 16ns-width.



**Note:** the above described configurability of both the self-trigger logic and the trigger request logic are supported only by AMC FPGA firmware releases > 0.1.

Previous firmware doesn't implement the register address 0x1n84 as well as the 0x1n70, the self-trigger is intended only as the over/under threshold signal and a trigger request is intended only as the OR of the self-triggers couple.

## LVDS I/O Trigger

LVDS I/O specific pins on the front panel dedicated connector can be programmed as trigger inputs and enabled to participate in the common trigger generation with other trigger sources. Refer to § **Front Panel LVDS I/Os** for details.

## Trigger Coincidence Level

Operating with the default firmware, the acquisition trigger is a board common trigger. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.



**Note:** From AMC FPGA firmware release > 0.1, it is possible to program the self-trigger logic as described in § **Self-Trigger**.

Enabling the coincidences is possible by writing at register address 0x810C:

- Bits[7:0] enable the trigger request signals to participate in the coincidence;
- Bits[23:20] set the coincidence window ( $T_{TVAW}$ ) linearly in steps of the Trigger clock (8 ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

Number of enabled trigger requests > Majority level

Supposing bits[7:0] = FF (i.e. all the 8 trigger request signals are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a board common trigger is issued whenever at least two of the enabled trigger requests are in coincidence within the programmed  $T_{TVAW}$ .

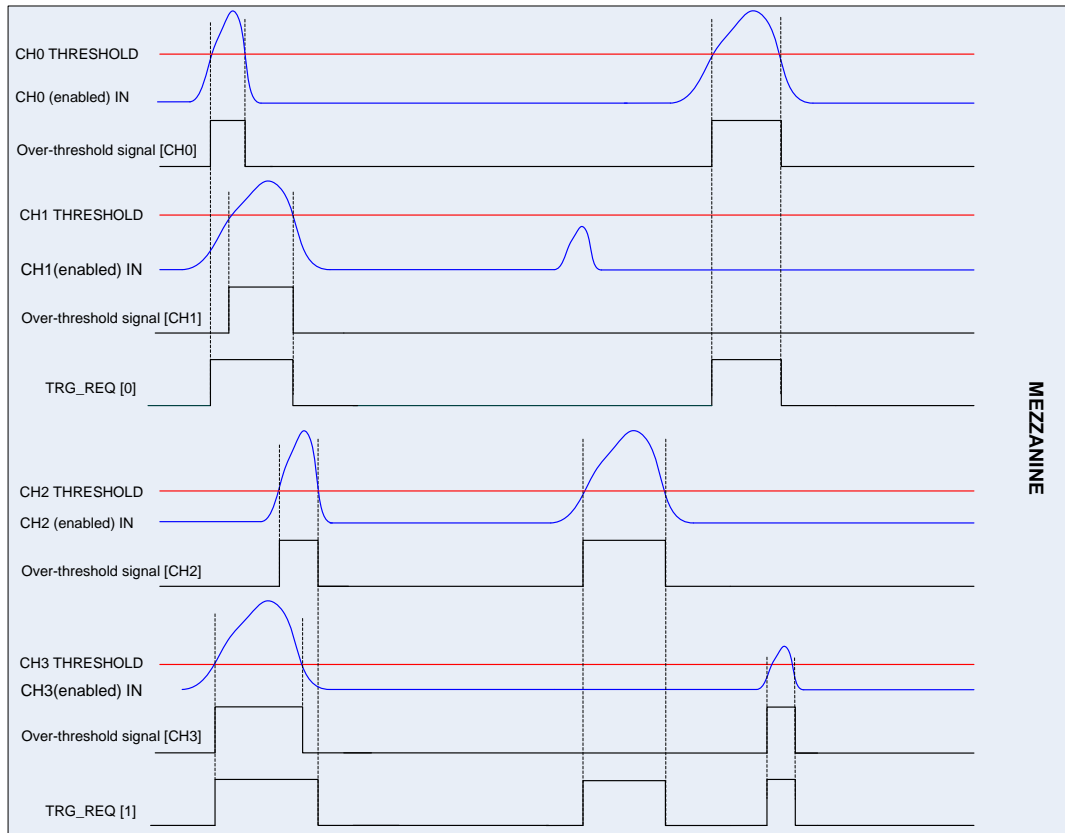
The Majority level must be smaller than the number of trigger request signals enabled via bits[7:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the  $T_{TVAW}$  is meaningless. In this case, the board common trigger is simple OR of the signals from the enabled channels pairs.



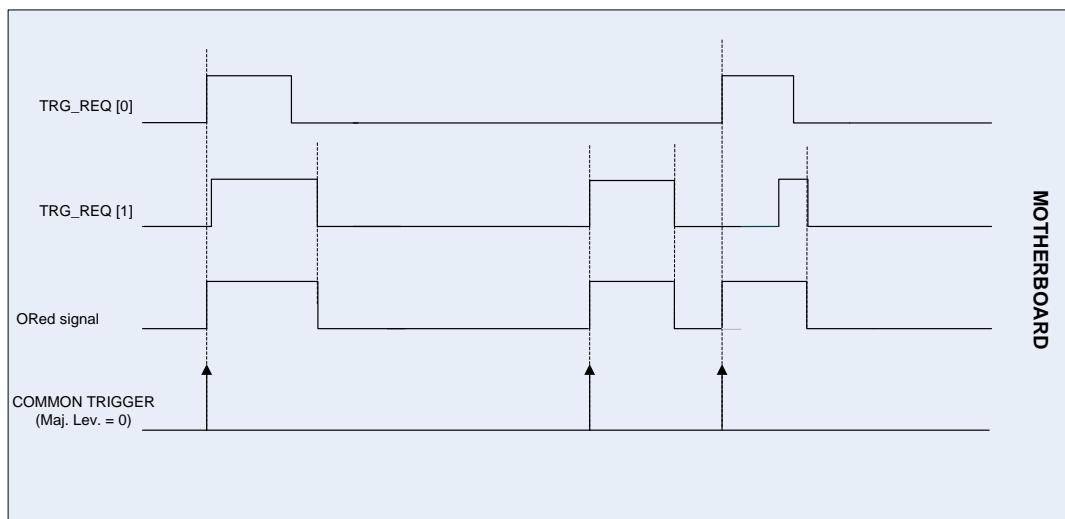


**Note:** In the following pictures CH4 up to CH15 are considered disabled in order not to overload the plots.

**Fig. 8.13** and **Fig. 8.14** show the trigger management in case the coincidences are disabled.

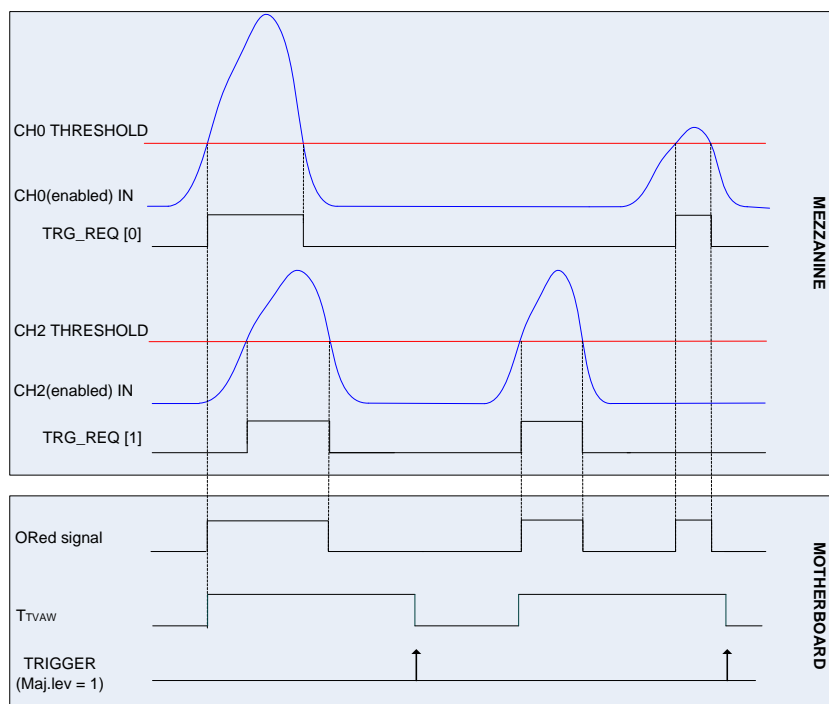


**Fig. 8.13:** Trigger request management at mezzanine level with Majority level = 0



**Fig. 8.14:** Trigger request management at motherboard level with Majority level = 0

**Fig. 8.15** and shows the trigger management in case the coincidences are enabled with Majority level = 1 and  $T_{TVAW}$  is a value different from 0. In order to simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH2.

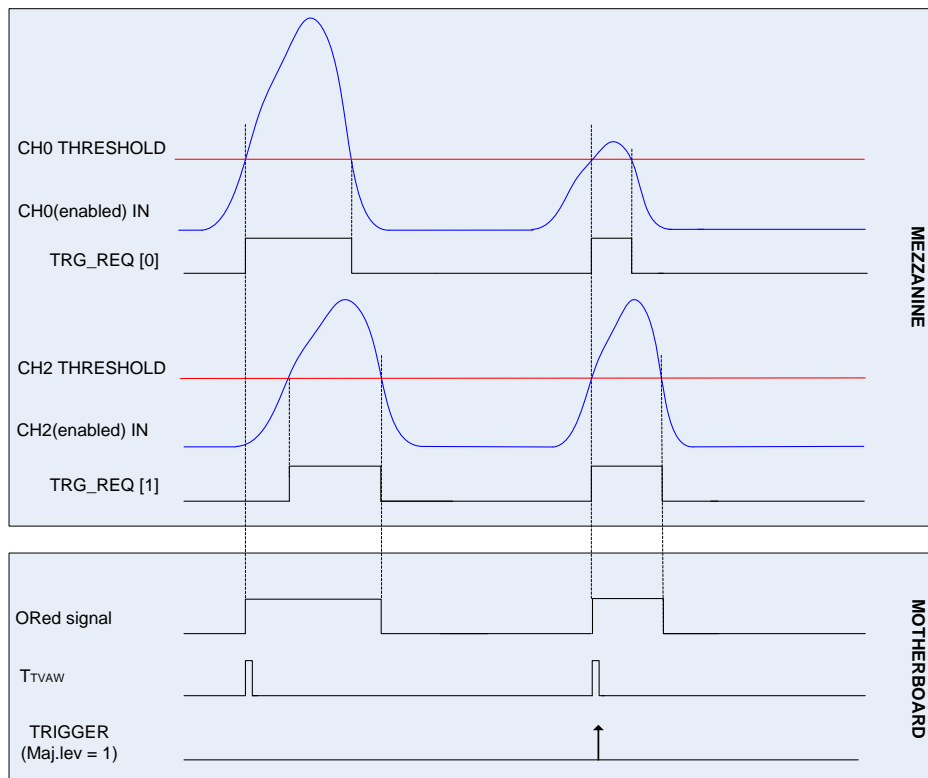


**Fig. 8.15:** Trigger request relationship with Majority level = 1 and  $T_{TVAW} \neq 0$



**Note:** with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

**Fig. 8.16** shows the trigger management in case the coincidences are enabled with Majority level = 1 and  $T_{TVAW} = 0$  (i.e. 1 clock cycle). In order to simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH2.



**Fig. 8.16:** Trigger request relationship with Majority level = 1 and  $T_{TVAW} = 0$

In this case, the common trigger is issued if at least two of the enabled trigger requests are instantaneously in coincidence (no  $T_{TVAW}$  is waited).



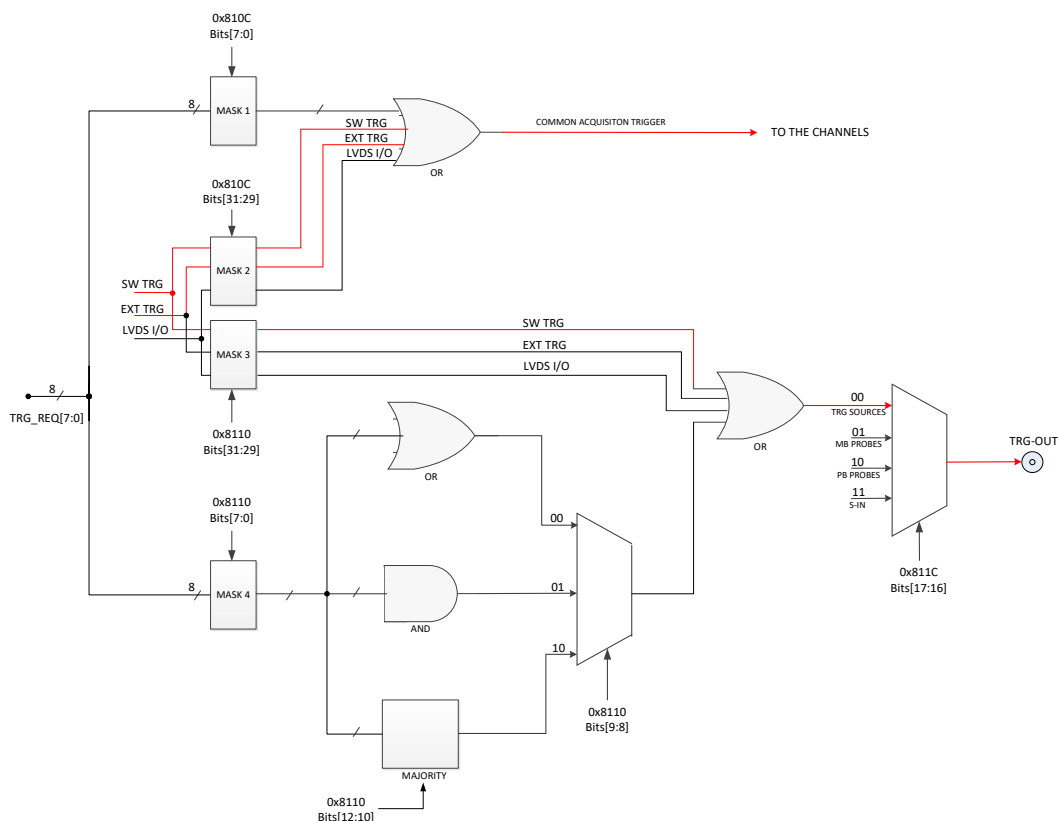
**Note:** a practical example of making coincidences with the digitizer in the standard operating is detailed in **[RD11]**.

## Trigger Distribution

As described in § **Trigger Management**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently provoking the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of **Fig. 8.17**).

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability (see **Fig. 8.17**), TRG-OUT can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of **Fig. 8.17**);
- the OR, AND or MAJORITY exclusively of the channel trigger requests.



**Fig. 8.17:** Trigger configuration of TRG-OUT front panel connector

The registers involved in the TRG-OUT programming are:

- Register address 0x8110;
- Register address 0x811C.



**Note:** Refer to **[RD3]** for registers complete description. Consider that, in case of 8-channel V1730B/VX1730B and V1725B/VX1725B versions, trigger requests and the relevant masks are over 4 bits instead of 8.

### Example

For instance, it could be required to start the acquisition on all the channels of a multi-board system as soon as one of the channels of a board (board “n”) crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V1495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are following described.

1. Register 0x8110 on board “n”:
  - Enable the desired trigger request as Trigger Out signal on board “n” (by bits[7:0] mask).
  - Disable Software Trigger, External Trigger and LVDS I/O Trigger as Trigger Out signal on board “n” (bits[31:29] = 000).
  - Set Trigger Out signal as the OR of the enabled trigger requests on board “n” (bits[9:8] = 00).
2. Register 0x811C on board “n”:
  - Configure the digitizer to propagates on TRG-OUT the internal trigger sources according to the 0x8110 settings (i.e. the enabled trigger request, in the specific case) on board “n” (bits[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board “n”):
  - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger, LVDS I/O Trigger and the Trigger Requests from the channels (bits[31:29] = 010; bits[7:0] = 00000000).

## Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards each one with Y channels, like if they were just one board with  $(N * Y)$  channels.

The main issue in the synchronization of a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board has to be chosen to be the “master” board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagation. This allows to have both the same ADC sampling clock, and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards is aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover, in case of busy state of one or more boards, the acquisition is inhibited for all boards.

For a detailed guide to multi-board synchronization, refer to **[RD2]**.

## Front Panel LVDS I/Os

The V1730 is provided with 16 general purpose programmable LVDS I/O signals (see § 6). In the default firmware, CAEN has developed for its digitizer series a new and more flexible configuration management that has been introduced from the release 3.8 of the ROC FPGA firmware and allows the LVDS I/Os signals to be programmed in terms of direction (INPUT/OUTPUT) and functionality by groups of 4. Only the description of the new configuration modes is given in this paragraph.

The new management is enabled by setting to 1 the bit[8] at register address 0x811C, that is set to 0 by default.

**THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES**

### **NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8**

*THE DEFAULT FIRMWARE OF V1730 MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN (see § 13) FOR INFORMATION.*

***SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!***

The direction of the signals are set by the bits[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]

Bit[3] → LVDS I/O[7:4]

Bit[4] → LVDS I/O[11:8]

Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.



**Note:** Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header Pattern field (see § **Event Structure**) the user can then choose to readout it or not

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	<i>Not available</i>	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: <i>reserved</i> 14: <i>reserved</i> 13: <i>reserved</i> 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	<i>Not available</i>	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: <i>reserved</i> 10: <i>reserved</i> 9: <i>reserved</i> 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	<i>Not available</i>	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: <i>reserved</i> 6: <i>reserved</i> 5: <i>reserved</i> 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	<i>Not available</i>	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: <i>reserved</i> 2: <i>reserved</i> 1: <i>reserved</i> 0: nClear_TTT

**Tab. 8.4:** Features description when LVDS group is configured as INPUT

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Ch[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Ch[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Ch[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Ch[3:0]	3: nRun 2: nTrigger 1: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

**Tab. 8.5:** Features description when LVDS group is configured as OUTPUT



## Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

## Mode 1: TRIGGER

Direction is INPUT: *Not available*.

Direction is OUTPUT: TrigOut\_Ch[3:0] are the trigger requests from the couples of channels CH0-CH1, CH2-CH3, CH4-CH5 and CH6-CH7, according to the logic described in § **Trigger Management**. Similarly, TrigOut\_Ch[7:4] are the trigger requests from the couples of channels CH8-CH9, CH10-CH11, CH12-CH13, and CH14-CH15.



**Note:** In case of 8-channel versions (V1730C and V1730D), trigger request outputs are limited to 4.

## Mode 2: nBUSY/nVETO

### nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

$$\text{Almost\_Full OR (LVDS\_BusyIn AND BusyIn\_enable)}$$

where

- **Almost\_Full** indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- **LVDS\_BusyIn** is available in nBUSY/nVETO configuration (see **Tab. 8.4**);
- **BusyIn\_enable** is set at register address 0x8100, bit[8].

### nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

### nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector or copy of the acquisition common trigger. This is selected by bit[16] of the 0x81A0 register.

### nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (register address 0x8100, bits[1:0] = 11). It is possible to program the Start on the level or on the edge of the nRunIn signal (register address 0x8100, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

## Mode 3: LEGACY

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

### **nClear\_TTT signal**

It is the only signal available as INPUT. It is the Trigger Time Tag (TTT) reset, like in the old configuration.

### **Busy Signal**

The Busy signal is active high and it is exactly the inverse of the nBusy signal (see § **Mode 2: nBUSY/nVETO**).

In case register address 0x816C is set to 0x0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.

### **DataReady Signal**

The DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

### **Trigger Signal**

The active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

### **Run Signal**

The Run signal is active high and represents the inverse of the nRun signal (see § **Mode 2: nBUSY/nVETO**).

## Analog Monitor

V1730 houses a 12-bit (100MHz) DAC with 0÷1 V dynamics on a 50  $\Omega$  load, whose input is controlled by the ROC FPGA and the signal output (driving 50  $\Omega$ ) is available on the MON/ $\Sigma$  output connector (see Fig. 2.1 and § 6). MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bits[2:0] at register address 0x8144:

- Trigger Majority Mode (*Monitor Mode* = 000)
- Test Mode (*Monitor Mode* = 001)
- Buffer Occupancy Mode (*Monitor Mode* = 011)
- Voltage Level Mode (*Monitor Mode* = 100)

### Trigger Majority Mode (*Monitor Mode* = 000)

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of channels under/over threshold (1 step = 125 mV); this allows, via an external discriminator, to produce a common trigger signal, as the number of triggering channels has exceeded a particular threshold.

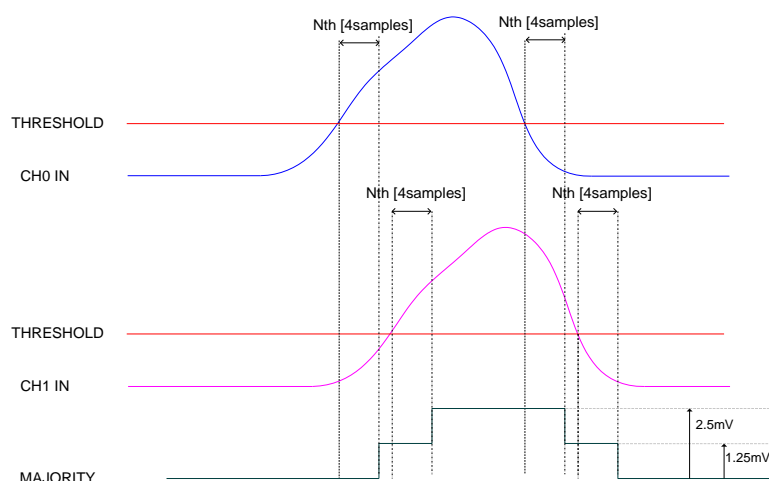


Fig. 8.18: Majority logic (2 channels over threshold; bit[6]= 0 at register address 0x8000)

### Test Mode (*Monitor Mode* = 001)

In this mode, the MON output provides a saw-tooth signal with 1-V amplitude and 24.41-kHz frequency.

### Buffer Occupancy Mode (*Monitor Mode* = 011)

In this mode, MON output connector provides a voltage value increasing proportionally with the number of buffers filled with events, in fixed steps of 0.976 mV given by

$$\frac{V_{\max}}{\text{Maximum\_Number\_of\_Buffers}}$$

where  $V_{\max} \sim 1$  V and *Maximum\_Number\_of\_Buffers* = 1024 (i.e. the value of register address 0x800C, as introduced in § Multi-Event Memory Organization).

**Example:** if 0x800C = 0x4 (i.e. 16 buffers), the maximum Buffer Occupancy output voltage level is given by  $0.976 \text{ mV} * 2^4$ .

This mode allows to test the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

### Voltage Level Mode (*Monitor Mode* = 100)

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written at register address 0x8138, with:  $V_{\text{mon}} = 1/4096 * N$  (Volt).

## Test Pattern Generator

The AMC FPGA can emulate the ADC and write into memory a ramp (0, 1, 2, 3,...FF, FF, FE..., 0) for test purposes. It can be enabled via register address 0x8000.

## Reset, Clear and Default Configuration

### Global Reset

Global Reset is performed at Power-ON of the module or via software by write access at register address 0xEF24 (whatever 32-bit value can be written). It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

### Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28 (whatever 32-bit value can be written).

### Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to the front panel Trigger Time Tag Reset input (see § **Front Panel LVDS I/Os**) or to the S-IN input (leading edge sensitive).

## VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

### Addressing Capabilities

- **Base address:** the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see Fig. 7.2), then it is validated only with either a Power-ON cycle or a System Reset (see § Global Reset).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

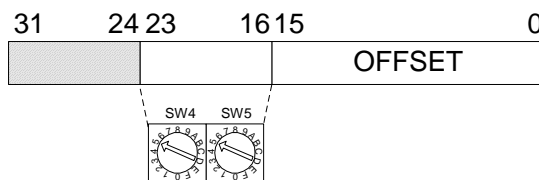


Fig. 8.19: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	-

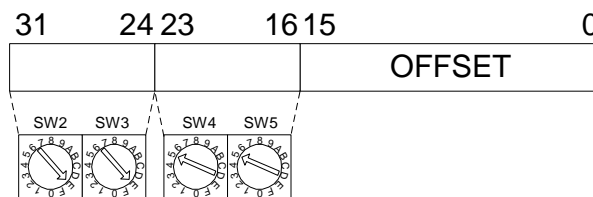


Fig. 8.20: A32 addressing

- **CR/CSR address:** the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

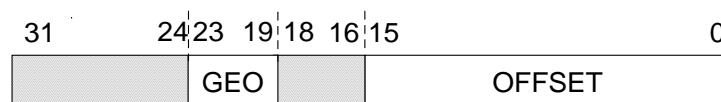
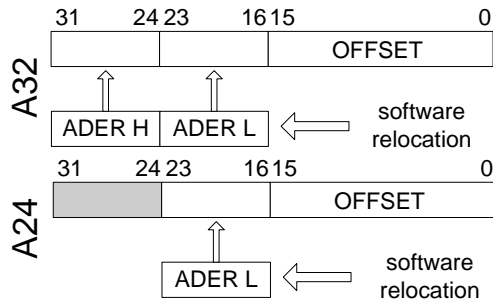


Fig. 8.21: CR/CSR addressing

## Address Relocation

Register address 0xEF10 (bits[15:0]) allows to set via software the board Base Address (valid values  $\neq 0$ ). Such register allows to overwrite the rotary switches settings; its setting is enabled via register address 0xEF00 (bit[6]). The used addresses are:



**Fig. 8.22:** Software relocation of base address

## Data Transfer Capabilities and Events Readout

V1730 and V1725 feature a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in § **Multi-Event Memory Organization**. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers. The acquisition process is so “dead timeless” until the memory becomes full (see § **Acquisition Synchronization**).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled channels (from 0 to 15) as reported in **Tab. 8.3**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels.

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

### Single D32 Transfer

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § **Event Structure**.

It is suggested, after the 1<sup>st</sup> word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read completely the event.

### Block Transfer D32/D64, 2eVME

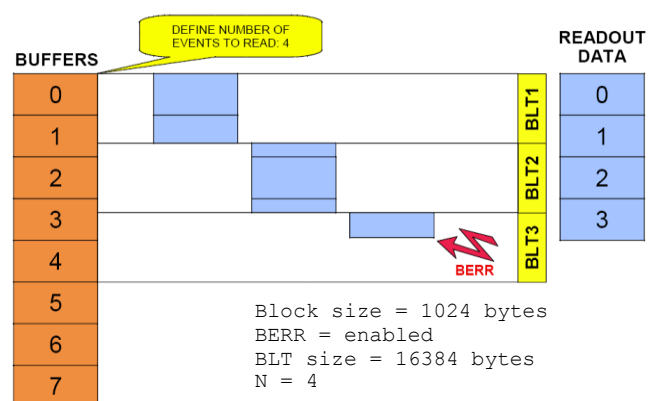
The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library (consult **[RD5]** at p. 19).

The event is configurable as indicated in the introduction of the paragraph, namely:

$$[\text{Event Size}] = [8 * (\text{Buffer Size})] + [16 \text{ bytes}]$$

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).



**Fig. 8.23:** Example of BLT readout

Since some 64-bit CPU cut off the last 32-bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at register address 0xEF00.

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle

## Chained Block Transfer D32/D64

The V1730 allows to readout events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT\_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).



## Optical Link Access

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight V1730/V1725 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two V1730/V1725 with the A3818 PCIe card. Detailed information on CAEN PCI/PCIe Controllers can be find at [www.caen.it](http://www.caen.it):

*Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controller*

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

Bit[3] at register address 0xEF00 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level (see "Interrupt Configuration" in [RD5]).

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously

# 9 Drivers & Libraries

## Drivers

In order to interface with the V1730/V1725, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows and Linux OS:

- **CONET Optical Link**, managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the “Software/Firmware” area at the A2818 or A3818 page (**login required**)



**Note:** For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

## Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, **the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer.**

The CAENDigitizer installation package and relevant documentation are available on CAEN website in the ‘Download’ area at the CAENDigitizer Library page.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm.**

The CAENComm installation package, the relevant documentation and the link to the required CAENVMELib, are available on CAEN website in the ‘Download’ area at the CAENComm Library page.

CAENComm (and so the CAENDigitizer) supports the following communication channels (**Fig. 9.1**):

PC → USB (V1718) → VMEbus → V1730/V1725

PC → PCI/PCIe (A2818/A3818) → CONET → V1730/V1725

PC → PCI/PCIe (A2818/A3818) → CONET (V2718) → VMEbus → V1730/V1725

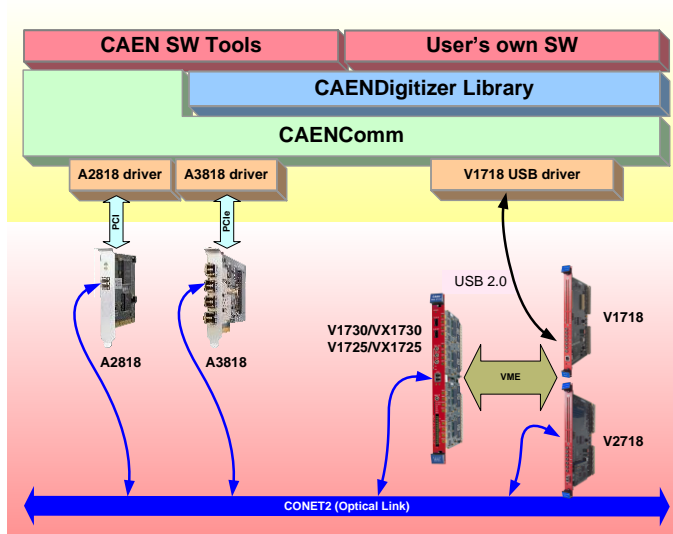


Fig. 9.1: Drivers and software layers

# 10 Software Tools

CAEN provides software tools to interface the V1730/V1725, which are available for [free download](#) on [www.caen.it](#) at:

*Home / Products / Firmware/Software / Digitizer Software*

## CAENUpgrader

CAENUpgrader is a free software composed of command line tools together with a Java Graphical User Interface.

Specifically for the V1730/V1725, CAENUpgrader allows in few easy steps to:

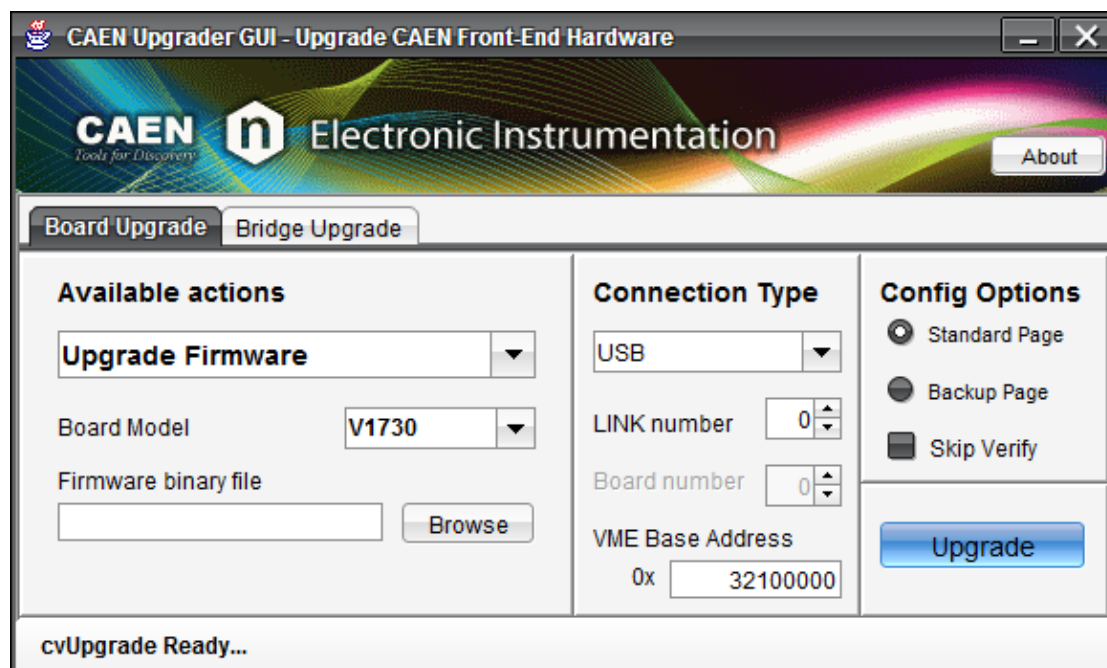
- Upload different FPGA firmware versions on the board
- Read the firmware release of the board and the bridge (when used)
- Manage the firmware license, in case of pay firmware
- Upgrade the internal PLL
- Get the Board Info file, useful in case of support

CAENUpgrader can operate with Windows and Linux, 32 and 64-bit OSs.

The program relies on the CAENComm and CAENVMELib libraries (see § 9) and requires third-party Java SE6 (or later) to be installed.



**Note:** Windows version of CAENUpgrader is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be already installed apart by the user.



**Fig. 10.1:** CAENUpgrader Graphical User Interface

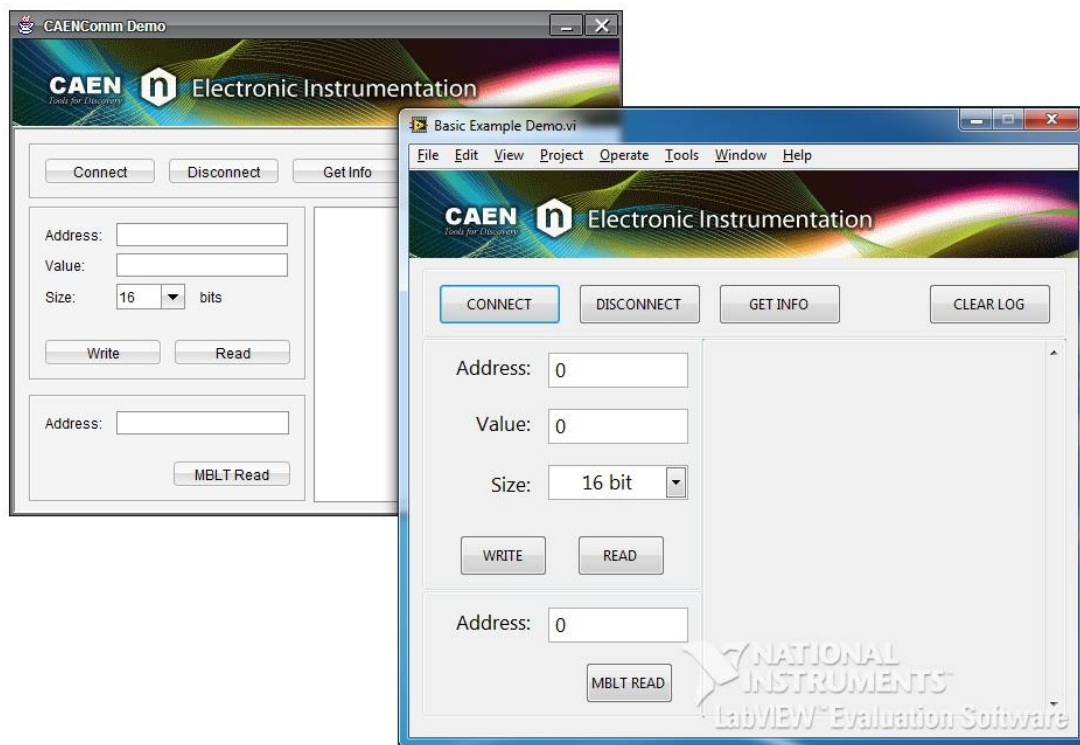
CAENUpgrader installation package can be downloaded on CAEN web site (**login required**) at:

*Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader*

The reference document for installation instructions and program detailed description is **[RD1]**, downloadable at the same page above, in the *Documentation* tab.

## CAENComm Demo

**CAENComm Demo** is a simple program developed in C/C++ source code and provided both with Java and LabVIEW GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.



**Fig. 10.2:** CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo can operate with Windows OSs, 32 and 64-bit. It requires CAENComm and CAEVMelib libraries as additional software to be installed (see § 9).

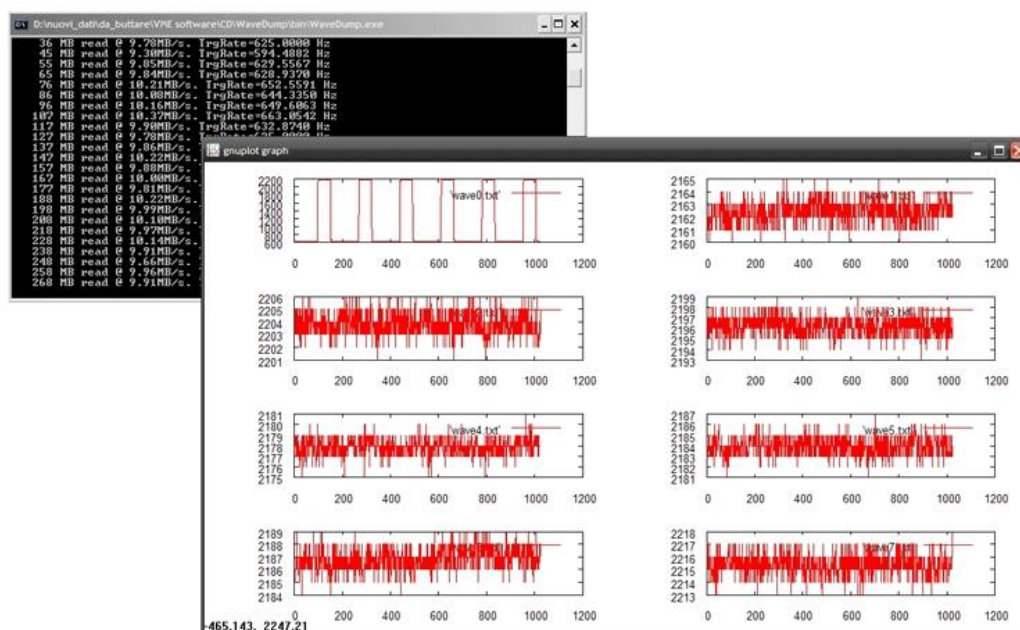
The Demo is included in the CAENComm library installation Windows package, which can be downloaded on CAEN web site (**login required**) at:

*Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library*

## CAEN WAVEDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the default firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: [www.gnuplot.info](http://www.gnuplot.info)).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.



**Fig. 10.3:** CAEN WaveDump

CAEN WaveDump can operate with Windows and Linux, 32 and 64-bit OSs.

The program relies on the CAENDigitizer, CAENComm and CAENVMElib libraries (see § 9). Linux users are required to install the third-party Gnuplot.



**Note:** Windows version of WaveDump is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be previously installed by the user.

The installation packages can be downloaded on CAEN web site (**login required**) at:

*Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAEN WaveDump*

The reference documents for installation instructions and program detailed description are **[RD6]** and **[RD7]**, downloadable at the same page above, in the *Documentation* tab.

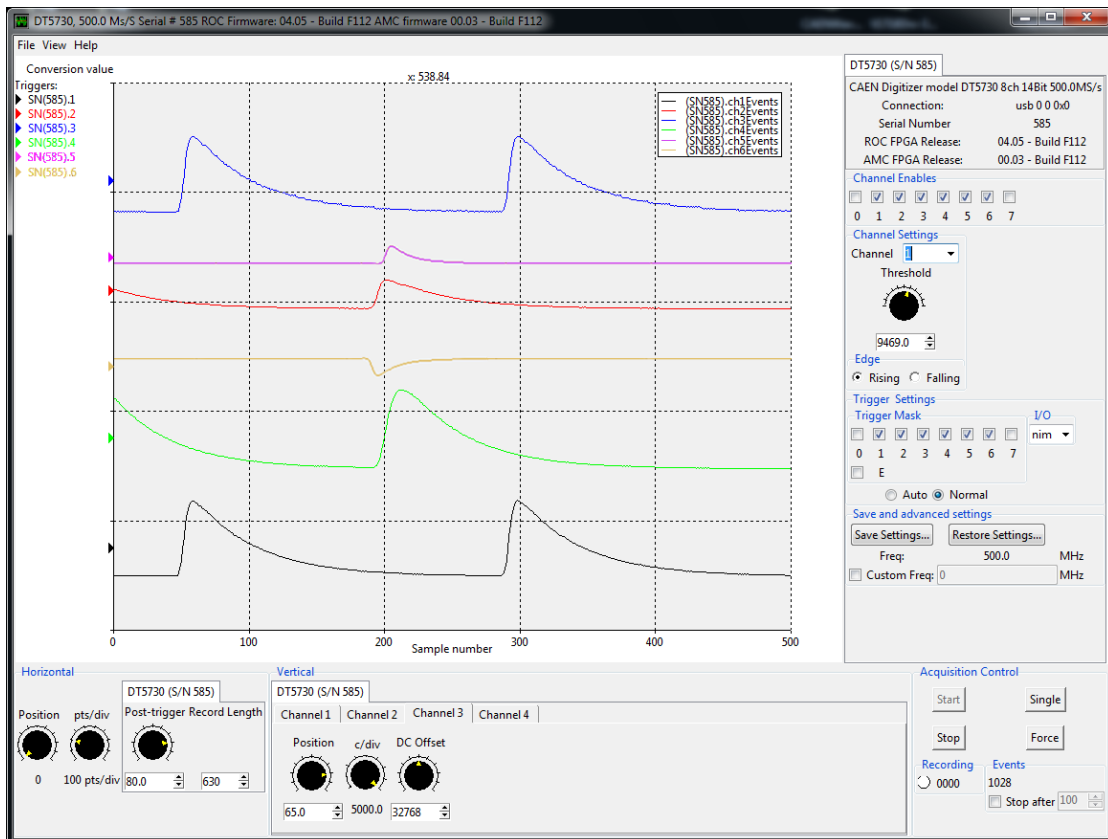
## CAENScope

In a brand new framework, CAENScope software implements the features of an easy-to-use digital oscilloscope to be used with CAEN digitizers running the default firmware.



**Note:** CAENScope support for 725 digitizer family is **COMING SOON**

CAENScope user friendly interface presents different sections to easily manage the digitizer configuration and plot the waveforms. Once connected, the program retrieves the digitizer information. Different parameters can be set for the channels, the trigger and the trace visualization (up to 12 traces can be simultaneously plotted). Signals are recordable to files in two different formats: Biary (SQLite db) and Text (XML). It is also possible to save and restore the program settings.



**Fig. 10.4:** CAENScope main frame

CAENScope can operate with Windows and Linux, 32 and 64-bit OSs. Linux users are required to install the following packages:

- sharutils;
- libXft;
- libXss (specifically for Debian derived distributions, e.g. Debian, Ubuntu, etc.);
- libXScrnSaver (specifically for RedHat derived distributions, e.g. RHEL, Fedora, Centos, etc.).

The program relies on the CAENDigitizer, CAENComm and CAENVMELib libraries.



**Note:** Windows version of CAENScope is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be previously installed by the user.

The installation packages can be downloaded on CAEN web site (**login required**) at:

*Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAENSCOPE*

The reference document for installation instructions and program detailed description is **[RD8]**, downloadable at the same page above, in the *Documentation* tab.

## DPP-PSD Control Software

The V1730 and V1725 can be equipped (on payment) with a special DPP-PSD firmware.

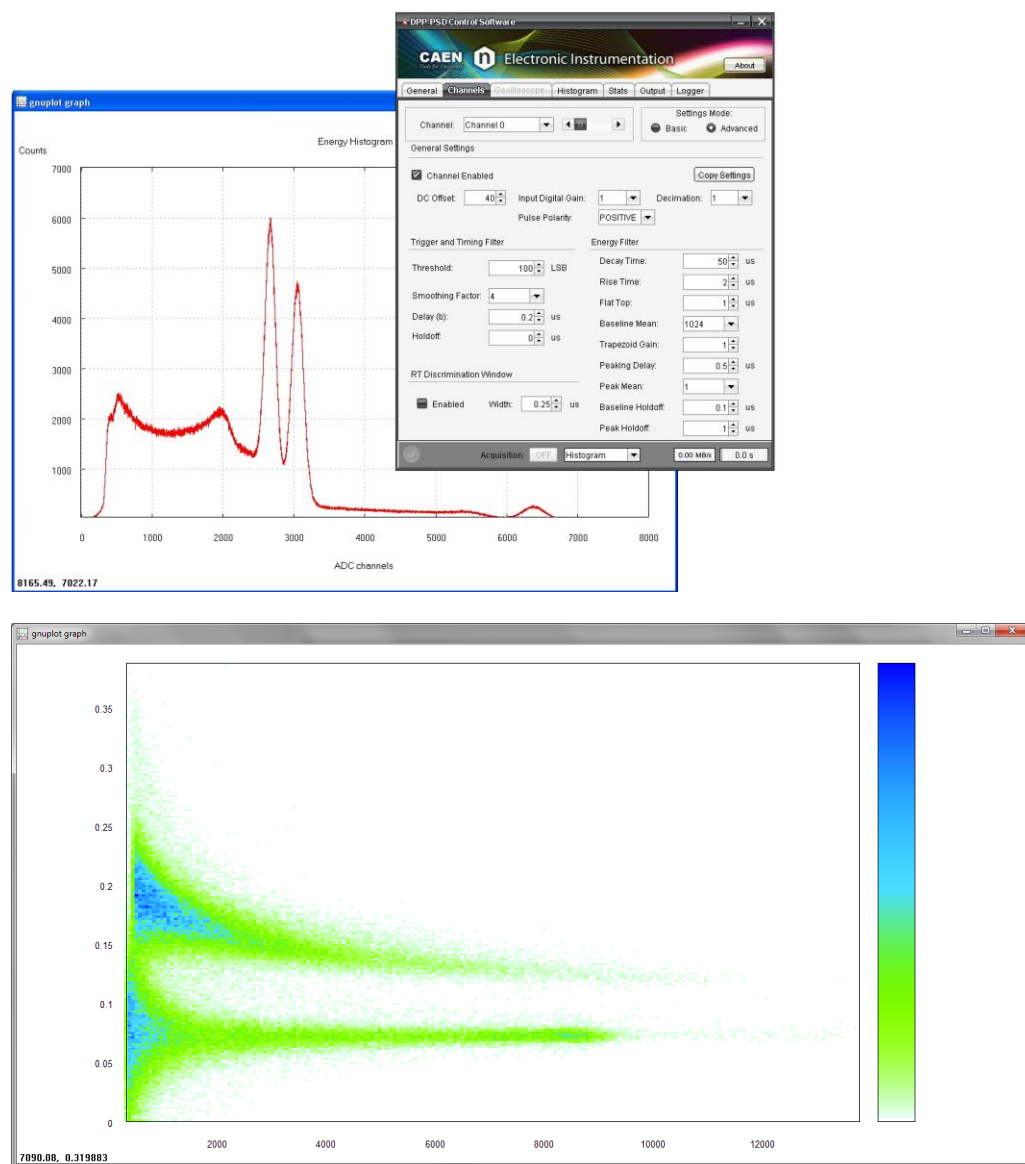
**DPP-PSD Control Software** is a software interface for configuration, acquisition and data plotting to be used with the digitizers who can run the DPP-PSD special firmware. It allows the user to set the parameters for the acquisition, to configure the DPP, to perform the data readout, the histogram collection and the spectrum or waveform plotting and saving. The program doesn't feature data analysis, but can be easily interfaced to software tools for offline analysis.

DPP-PSD Control Software is available both for Windows and Linux platforms.

The program relies on the CAENDigitizer, CAENComm and CAENVMELib libraries (see § 9). Third-party Java SE6 (or later) needs to be installed.



**Note:** Windows version of DPP-PSD Control Software is stand-alone (the required libraries are installed locally with the program; only the communication driver must be installed apart by the user), while the version for Linux needs the required libraries to be previously installed by the user.



**Fig. 10.5:** DPP-PSD Control Software: Top – DPP settings Tab and typical  $^{60}\text{Co}$  Total Charge Spectrum; Bottom - PSD 2-D Scatter Plot

The installation package can be downloaded on CAEN web site ([www.caen.it](http://www.caen.it)) at:

*Home / Products / Firmware/Software / Digitizer Software / Readout Software / DPP-PSD Control Software*

The reference document for installation instructions and program detailed description is [RD9].



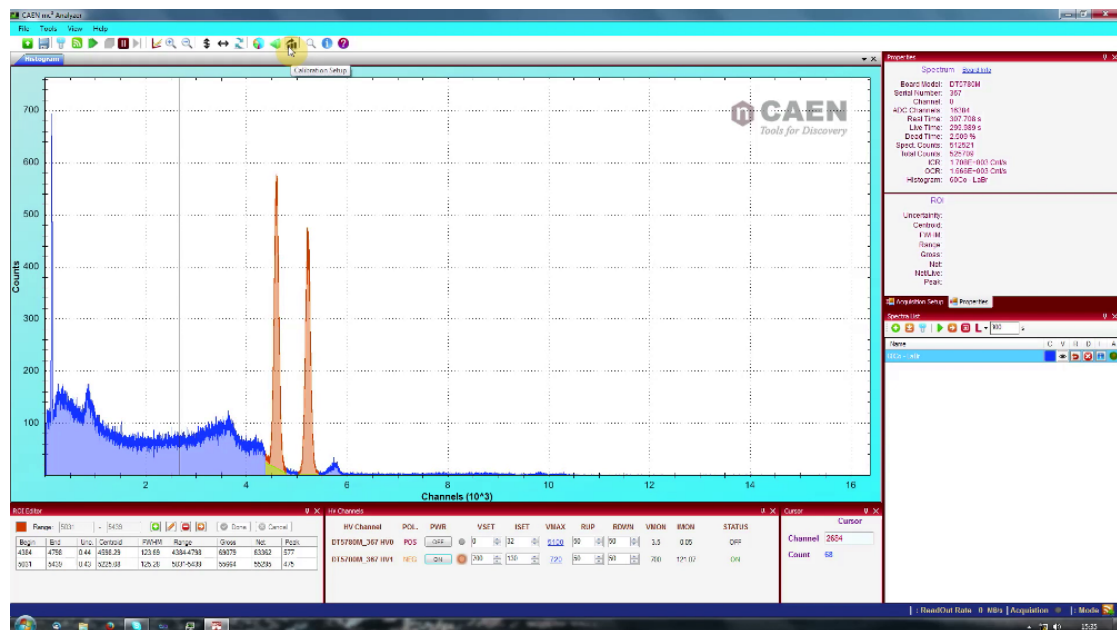
## MC<sup>2</sup>Analyzer (MC<sup>2</sup>A)

MC<sup>2</sup>Analyzer (MC<sup>2</sup>A) is a software specifically designed for digitizers running the special DPP-PHA firmware (724, 725 and 730 families) and the Digital MCAs (x780 Dual Digital MCA, x781 Dual/Quad Digital MCA, DT5770).

The software is able to completely control and manage a set of boards acquiring data simultaneously, making therefore a multi-board system a "Multichannel - Multichannel Analyzer".

MC<sup>2</sup>A allows the user to set all the relevant DPP-PHA parameters for each acquisition channel (like trigger threshold, shaping parameters, etc.), handle the communication with the connected boards, run the data acquisition and plot both waveforms for on-line monitoring of the acquisition and histograms. It can also control the HV power supplies provided in the x780.

Moreover, it is able to perform advanced mathematical analysis on both the ongoing histograms and collected spectra: peak search, background subtraction, peak fitting, energy calibration, ROI selection, dead time compensation, histogram rebin and other features available.



**Fig. 10.6:** MC<sup>2</sup>Analyzer (MC<sup>2</sup>A) software tool

MC<sup>2</sup>Analyzer is currently available only for Windows platforms. The installation package can be downloaded on CAEN web site ([www.caen.it](http://www.caen.it)):

*Home / Products / Firmware/Software / Digitizer Software / Readout Software*

The reference document for installation instructions and program detailed description is **[RD10]**.



**Note:** Windows version of MC<sup>2</sup>Analyzer is stand-alone (the required libraries are installed locally with the program; only the communication driver must be installed apart by the user).



# 11 HW Installation

- The V1730/V1725 fits into 6U VME crates.
- **The V1730 cannot be operated with CAEN crates VME8001/8002/8004.**
- VX1730/VX1725 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

**CAUTION:** this product needs proper cooling:



**USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!**

CAEN HEARTLY RECOMMEND TO MONITOR THE TEMPERATURE OF THE ADC CHIPS DURING THE BOARD OPERATION BY READING AT REGISTER ADDRESS 0x1nA8 (SEE **[RD3]** FOR DETAILS)



**V1730/VX1730 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!**

**CAUTION:** this product needs proper handling.



**ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!**

## Power-on Sequence

To power on the board, follow this procedure:

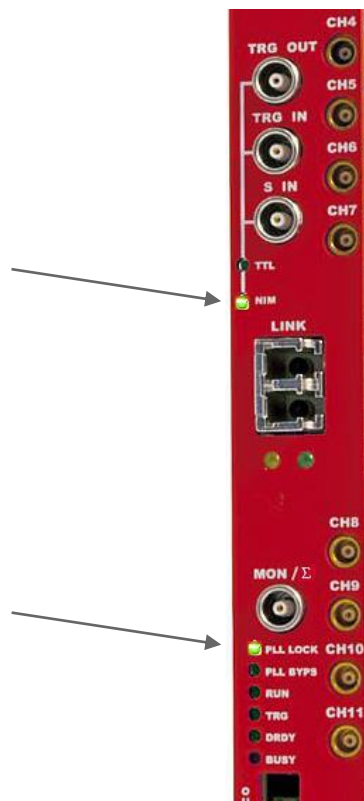
1. Insert the V1730/V1725 into the crate;
2. power up the crate.

## Power-on Status

At power-on the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power-on, the front panel LEDs status is that only the NIM and PLL LOCK remain ON (see **Fig. 11.1**).



**Fig. 11.1:** Front panel LEDs status at power ON

**AFTER POWER-ON, CAEN RECOMMENDS TO PERFORM THE CHANNEL CALIBRATION AS DESCRIBED AT PAGE 27 IN ORDER TO ACHIEVE THE BEST DEVICE PERFORMANCE**

## 12 Firmware and Upgrades

The board hosts one FPGA on the mainboard and four FPGAs on the mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

**ROC FPGA MAINBOARD FPGA** (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

**AMC FPGA MEZZANINE FPGA** (ADC readout/Memory Controller):

FPGA Altera Cyclone EP4CE30

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of default firmware, the board is delivered equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one by default in normal operating.

VME digitizers in the 730 and 725 families are equipped with an on-board dedicated SW1 dip switch, set on STD position by default, allowing to select the first FLASH page to be read at power-on (see § **Internal Components**).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see § 10).

***IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!***

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page) if this is not corrupted as well. The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

***BECAUSE OF AN UPGRADE FAILURE, THE SW1 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs***

At power-on, if the user cannot communicate with the board, it needs to be sent back to CAEN in repair (see § 13).

## Default Firmware Upgrade

The V1730 and V1725 are delivered running a default firmware to operate the board for waveform recording.

The default firmware updates are available for download on CAEN website ([www.caen.it](http://www.caen.it)) in the *Software/Firmware* tab at the V1730/V1725 web page (**login required**):

*Home / Products / Modular Pulse Processing Electronics / VME / Digitizers / V1730 (or V1725)*

## Default Firmware File Description

The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the default firmware files compatible with one or more digitizer families.

CFA and its name follows this general scheme:

x730\_revX.Y\_W.Z.CFA

x725\_revX.Y\_W.Z.CFA

where:

- x730 (x725) are all the supported boards: DT5730 (DT5725), N6730 (N6725), V1730 (V1725), VX1730 (VX1725)
- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel FPGA

## DPP Firmware Upgrade

CAEN can provides V1730 and V1725 with special DPP-PSD and DPP-PHA firmware for Physics Applications. The digitizer running DPP-PSD firmware becomes a digital replacement of dual gate QDC, discriminator and gate generator. The digitizer running DPP-PHA firmware becomes a digital replacement of Shaping Amplifier and Peak Sensing ADC (Multi-Channel Analyzer) by means of digital trapezoidal filters.

- The DPP-PSD firmware updates are available for download on CAEN website in the *Download* tab (**login required**) at:

*Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-PSD*

- The DPP-PHA firmware updates are available for download on CAEN website in the *Download* tab (**login required**) at:

*Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-PHA*

## DPP Firmware File Description

The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the firmware files compatible with the same DPP firmware and family of digitizers.

CFA and its name follows this general scheme:

x730\_DPP-PSD\_rev\_X.Y\_136.Z.CFA

x725\_DPP-PSD\_rev\_X.Y\_136.Z.CFA

x730\_DPP-PHA\_rev\_X.Y\_139.Z.CFA

x725\_DPP-PHA\_rev\_X.Y\_139.Z.CFA

where the major revision number of the channel FPGA (136 or 139) is fixed for the specific DPP algorithm and digitizer family. The other fields have the same meaning as in the default firmware file description.



**Note:** DPP special firmware is a pay firmware requiring a license to be purchased. If not licensed, the firmware can be loaded but it will run fully functional with a time limitation per power cycle (30 minutes). Details on the license ordering procedure can be found in [RD1].



**Note:** if the DPP firmware license is included in the same order of a V1730 (V1725), the customer will be delivered with the digitizer already running the licensed (i.e. unlocked) special firmware. Once unlocked, upgrading the same kind of DPP firmware requires no further licensing.

## 13 CAEN Support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at [www.caen.it](http://www.caen.it).

### Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.

Contacts for shipping are reported on the website at *Home / Contacts*.

### Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

[support.nuclear@caen.it](mailto:support.nuclear@caen.it)  
(for questions about the hardware)

[support.computing@caen.it](mailto:support.computing@caen.it)  
(for questions about software and libraries)



CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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