



User Manual UM5918

## 724 Family

Waveform Recording Firmware Registers

Rev. 2 - January 25<sup>th</sup>, 2018

# Purpose of this Manual

The User Manual contains the full description of the Waveform Recording firmware registers for 724 digitizer family. The description is compliant with the firmware revision **4.17\_0.15**.

For future release compatibility check in the firmware history files.

## Change Document Record

Date	Revision	Changes
April 18 <sup>th</sup> , 2017	00	First release unified for 724 digitizer family
October 5 <sup>th</sup> , 2017	01	Updated 0x8100, 0x8170 and 0xEF04 registers. Added 0x81C4 register.
January 25 <sup>th</sup> , 2018	02	Updated bit[15] of 0x1n80. Modified register 0x8170. Updated bit[3:0] of 0x8178 (reserved). Added a note to register 0x81C4.

## Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

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# Index

<b>Purpose of this Manual</b> . . . . .	<b>2</b>
<b>Change document record</b> . . . . .	<b>2</b>
<b>Symbols, abbreviated terms and notation</b> . . . . .	<b>2</b>
<b>1 Registers and Data Format</b> . . . . .	<b>5</b>
Reset and Clear . . . . .	5
Register Address Map . . . . .	6
Event Readout Buffer . . . . .	9
Zero Suppression Threshold . . . . .	10
Zero Suppression Samples . . . . .	11
Channel n Trigger Threshold . . . . .	12
Time Over/Under Threshold . . . . .	13
Channel n Status . . . . .	14
AMC Firmware Revision . . . . .	15
DC Offset . . . . .	16
Board Configuration . . . . .	17
Buffer Organization . . . . .	18
Custom Size . . . . .	19
Inspection Mode Polarity and Shift . . . . .	20
Decimation Factor . . . . .	21
Acquisition Control . . . . .	22
Acquisition Status . . . . .	24
Software Trigger . . . . .	25
Global Trigger Mask . . . . .	26
Front Panel TRG-OUT (GPO) Enable Mask . . . . .	27
Post Trigger . . . . .	28
LVDS I/O Data . . . . .	29
Front Panel I/O Control . . . . .	30
Channel Enable Mask . . . . .	33
ROC FPGA Firmware Revision . . . . .	34
Event Stored . . . . .	35
Voltage Level Mode Configuration . . . . .	36
Software Clock Sync . . . . .	37
Board Info . . . . .	38
Analog Monitor Mode . . . . .	39
Event Size . . . . .	40
Inspection Mode Configuration . . . . .	41
Fan Speed Control . . . . .	42
Memory Buffer Almost Full Level . . . . .	43
Run/Start/Stop Delay . . . . .	44
Board Failure Status . . . . .	45
Front Panel LVDS I/O New Features . . . . .	46
Buffer Occupancy Gain . . . . .	47
Extended Veto Delay . . . . .	48
Readout Control . . . . .	49
Readout Status . . . . .	50
Board ID . . . . .	51
MCST Base Address and Control . . . . .	52
Relocation Address . . . . .	53
Interrupt Status/ID . . . . .	54

Interrupt Event Number . . . . .	55
Max Number of Events per BLT . . . . .	56
Scratch . . . . .	57
Software Reset . . . . .	58
Software Clear . . . . .	59
Configuration Reload . . . . .	60
Configuration ROM Checksum . . . . .	61
Configuration ROM Checksum Length BYTE 2 . . . . .	62
Configuration ROM Checksum Length BYTE 1 . . . . .	63
Configuration ROM Checksum Length BYTE 0 . . . . .	64
Configuration ROM Constant BYTE 2 . . . . .	65
Configuration ROM Constant BYTE 1 . . . . .	66
Configuration ROM Constant BYTE 0 . . . . .	67
Configuration ROM C Code . . . . .	68
Configuration ROM R Code . . . . .	69
Configuration ROM IEEE OUI BYTE 2 . . . . .	70
Configuration ROM IEEE OUI BYTE 1 . . . . .	71
Configuration ROM IEEE OUI BYTE 0 . . . . .	72
Configuration ROM Board Version . . . . .	73
Configuration ROM Board Form Factor . . . . .	74
Configuration ROM Board ID BYTE 1 . . . . .	75
Configuration ROM Board ID BYTE 0 . . . . .	76
Configuration ROM PCB Revision BYTE 3 . . . . .	77
Configuration ROM PCB Revision BYTE 2 . . . . .	78
Configuration ROM PCB Revision BYTE 1 . . . . .	79
Configuration ROM PCB Revision BYTE 0 . . . . .	80
Configuration ROM FLASH Type . . . . .	81
Configuration ROM Board Serial Number BYTE 1 . . . . .	82
Configuration ROM Board Serial Number BYTE 0 . . . . .	83
Configuration ROM VCXO Type . . . . .	84

# 1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

## Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register
- by hardware (VME boards only), through the LVDS interface properly configured (see the section "Front Panel LVDS I/Os" of the digitizer User Manual).

## Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

- R     **Read only.** The register can be accessed in read only mode.  
W     **Write only.** The register can be accessed in write only mode.  
R/W   **Read and write.** The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

- I     **Individual register.** This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual.  
Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example:
- access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board;
  - to write the same value for all channels in the board, access to 0x8070 (broadcast write).  
To read the corresponding value, access to the individual address 0x1n70.
- C     **Common register.** Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Event Readout Buffer	0x0000 - 0x0FFC	R	C
Zero Suppression Threshold	0x1n24, 0x8024	R/W	I
Zero Suppression Samples	0x1n28, 0x8028	R/W	I
Channel n Trigger Threshold	0x1n80, 0x8080	R/W	I
Time Over/Under Threshold	0x1n84, 0x8084	R/W	I
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Buffer Organization	0x800C	R/W	C
Custom Size	0x8020	R/W	C
Inspection Mode Polarity and Shift	0x802A	R/W	C
Decimation Factor	0x8044	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
Post Trigger	0x8114	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Event Stored	0x812C	R	C
Voltage Level Mode Configuration	0x8138	R/W	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Analog Monitor Mode	0x8144	R/W	C
Event Size	0x814C	R	C
Inspection Mode Configuration	0x8150	R/W	C
Fan Speed Control	0x8168	R/W	C
Memory Buffer Almost Full Level	0x816C	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Buffer Occupancy Gain	0x81B4	R/W	C
Extended Veto Delay	0x81C4	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Max Number of Events per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C

Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C



## Event Readout Buffer

This is the addressment space for the event readout. The event is a series of 32-bit words according to the event structure defined in the digitizer User Manual.

Address        0x0000 - 0x0FFC  
Mode            R  
Attribute       C

Bit	Description
[31:0]	32-bit word of the event.

## Zero Suppression Threshold

This register defines the threshold and the operation logic (over/under threshold) for the zero suppression.

In case of "Full Suppression based on the integral", the threshold is compared with the sum of the event samples within the acquisition window (i.e. the integral). The event is acquired if the integral is higher/lower than the threshold value, otherwise it is discarded.

In case of "Full Suppression based on the amplitude", the threshold is compared with the height of each sample of the event. The event is acquired if its samples are over/under threshold for at least  $N_s$  samples as defined in 0x1n28.

In case of "Zero Length Encoding", the threshold is compared with the height of each sample in the event. Samples over/under threshold are defined as "good" samples and flagged in the data. The other samples are flagged as "skipped" and discarded; in the data it is reported the number of skipped samples only. It is also possible to define the number of samples to be acquired before and after the over/under threshold through register 0x1n28.

Address	0x1n24, 0x8024
Mode	R/W
Attribute	I

Bit	Description
[29:0]	Threshold for the Zero Suppression (expressed as an absolute value in the ADC scale). NOTE: In case of "Full Suppression based on the amplitude" and "Zero Length Encoding" only bits[13:0] are significant and bits[29:14] are reserved.
[30]	Threshold Weight (used for "Full Suppression based on the integral" only). Options are: 0 = Fine threshold step (Threshold = bits[29:0] of this register); 1 = Coarse threshold step (Threshold = bits[29:0] · 64).
[31]	Operation logic. Options are: 0 = positive logic. The condition is met when the data is over threshold; 1 = negative logic. The condition is met when the data is under threshold.

## Zero Suppression Samples

This register defines the number of samples for the zero suppression conditions.

In case of "Full Suppression based on the amplitude", it corresponds to the number  $N_s$  of subsequent samples over/under threshold necessary to validate the event.

In case of "Zero length encoding", this register sets both the samples to be acquired before and after the over/under threshold ( $N\_LBK$  and  $N\_LFWD$  respectively).

Address	0x1n28, 0x8028
Mode	R/W
Attribute	I

Bit	Description
[31:0]	In case of "Full Suppression based on the amplitude": number of samples over/under threshold for the zero suppression condition. Minimum value is 1. In case of "Zero Length Encoding": bits[15:0] = $N\_LFWD$ ; bits[31:16] = $N\_LBK$ .

## Channel n Trigger Threshold

The channel is able to generate a self-trigger signal when the digitized input pulse exceeds a configurable threshold Vth. This register allows to set Vth individually for each channel.

Address        0x1n80, 0x8080  
 Mode         R/W  
 Attribute     I

Bit	Description
[13:0]	Vth = Trigger Threshold Value expressed in LSB (default value is 0). 1 LSB = Input Dynamic Range / $2^{14\text{bit}}$ .
[14]	Reserved
[15]	Channel Trigger Polarity. Options are: 0 = positive; 1 = negative. This bit is in logic OR with bit[6] of register 0x8000: to set the individual trigger polarity, bit[6] at 0x8000 must be 0, then bit[15] at 0x1n80 must be 1 to set negative polarity for channel n. Example: positive polarity for all the channels but channel 2 and 3; the settings are: 0x8000 -> Bit[6] = 0 0x1280 -> bit[15] = 1 0x1380 -> bit[15] = 1
[31:16]	Reserved

## Time Over/Under Threshold

Each channel can generate a local trigger at the threshold crossing (as defined in register 0x1n80). This register defines how many samples the signal has to remain over/under threshold to generate a trigger. Once this condition is met, the local trigger is delayed by the amount defined in this register with respect to the input signal, i.e. the trigger is at the end of the time over/under threshold.

Address        0x1n84, 0x8084  
Mode            R/W  
Attribute       I

Bit	Description
[11:0]	Number of samples over/under threshold according to the formula $N_s = N \cdot 4$ , where N is the register content. Each sample corresponds to 10 ns.
[31:12]	Reserved.

## Channel n Status

This register contains the status information of channel n.

Address        0x1n88  
 Mode         R  
 Attribute     I

Bit	Description
[0]	Memory Full.
[1]	Memory Empty.
[2]	Channel n DAC Busy. Options are: 0 = DC offset updated; 1 = Busy.
[31:3]	Reserved

## AMC Firmware Revision

This register contains the channel FPGA (AMC) revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 1.03, November 12th, 2007 is 0x7B120103.

EXAMPLE 2: revision 2.09, March 7th, 2016 is 0x03070209.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address            0x1n8C

Mode                R

Attribute          I

Bit	Description
[7:0]	AMC Firmware Minor Revision Number (Y).
[15:8]	AMC Firmware Major Revision Number (X).
[31:16]	AMC Firmware Revision Date (Y/M/DD).

## DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to  $2^{N_{Bit}} - 1$ , where  $N_{Bit}$  is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the  $N_{Bit}$  value and the board type.

Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.

**WARNING:** before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit.
[31:16]	Reserved.



## Board Configuration

This register contains general settings for the board configuration.

Address        0x8000, 0x8004 (BitSet), 0x8008 (BitClear)  
 Mode            R/W  
 Attribute       C

Bit	Description
[0]	Reserved: must be 0.
[1]	Trigger Overlap Setting (default value is 0). When two acquisition windows are overlapped, the second trigger can be either accepted or rejected. Options are: 0 = Trigger Overlapping Not Allowed (no trigger is accepted until the current acquisition window is finished); 1 = Trigger Overlapping Allowed (the current acquisition window is prematurely closed by the arrival of a new trigger).
[2]	Reserved: must be 0.
[3]	Test Pattern Enable (default value is 0). This bit enables a triangular (0<-->3FFF) test wave to be provided at the ADCs input for debug purposes. Options are: 0 = disabled; 1 = enabled.
[4]	Reserved: must be 1.
[5]	Reserved: must be 0.
[6]	Self-trigger Polarity (default value is 0). Options are: 0 = Positive (the self-trigger is generated upon the input pulse over-threshold); 1 = Negative (the self-trigger is generated upon the input pulse under-threshold).
[7]	When the Inspection mode is enabled (bits[2:0] = 010 of register 0x8144), this bit enables the propagation of the CHx DATA from the channel to the mother board ROC FPGA. Options are: 0 = CHx DATA propagation disabled (default); 1 = CHx DATA propagation enabled.
[15:8]	Reserved.
[19:16]	Selects the Zero Suppression algorithm. Options are: 0000 = no zero suppression (default); 0001 = full suppression based on the integral (ZS_INT); 0010 = zero length encoding (ZLE); 0011 = full suppression based on the amplitude (ZS_AMP).
[31:20]	Reserved.

## Buffer Organization

Sets the number of buffers in which the channel memory can be divided. A write access to this register causes a software clear.

According to the BUFFER\_CODE value written in the register, the number of buffers  $N_b$  is given by  $2^{\text{BUFFER\_CODE}}$ . The following table summarizes the memory size and the number of samples of one buffer, where  $k = 1024$  and  $M = 1024 \cdot 1024$ :

Register Value BUFFER_CODE	Number of Buffers ( $N_b$ )	Size of one Buffer	
		SRAM 1 MB/ch (512 kS)	SRAM 8 MB/ch (4 MS)
0x0	1	1 MB/ch (512 kS)	8 MB/ch (4 MS)
0x1	2	512 kB/ch (256 kS)	4 MB/ch (2 MS)
0x2	4	256 kB/ch (128 kS)	2 MB (1 MS)
0x3	8	128 kB/ch (64 kS)	1 MB/ch (512 kS)
0x4	16	64 kB/ch (32 kS)	512 kB/ch (256 kS)
0x5	32	32 kB/ch (16 kS)	256 kB/ch (128 kS)
0x6	64	16 kB/ch (8 kS)	128 kB/ch (64 kS)
0x7	128	8 kB/ch (4 kS)	64 kB/ch (32 kS)
0x8	256	4 kB/ch (2 kS)	32 kB/ch (16 kS)
0x9	512	2 kB/ch (1 kS)	16 kB/ch (8 kS)
0xA	1024	1 kB/ch (512 S)	8 kB/ch (4 kS)

To obtain a number of samples per buffer (referring to one channel) different from the table above, it is necessary to use the register address 0x8020. In this case, the BUFFER\_CODE must be set to have the closest buffer size with a number of samples per buffer larger than the one set by 0x8020.

EXAMPLE: to have a desired number of samples per buffer of 9000 (set through 0x8020), the BUFFER\_CODE must be 0x5 in case of 512kS/ch memory or 0x8 if 4MS/ch one.

WARNING: This register must not be written while acquisition is running.

Address      0x800C  
Mode         R/W  
Attribute    C

Bit	Description
[3:0]	BUFFER_CODE
[31:4]	Reserved.

## Custom Size

Writing the number of memory locations per event (N\_LOC) in this register, the user can set the record length, which is the number of samples (Ns) of the digitized waveform in the acquisition window.

WARNING: this register must not be written while acquisition is running.

Address        0x8020  
Mode            R/W  
Attribute       C

Bit	Description
[31:0]	Number of Memory Locations per Event (N_LOC). Options are: 0 = Custom Size disabled (record length is given by the register address 0x800C); N_LOC = the number of samples of the record length is this given by the formula $N_s = N\_LOC \cdot 2$ . EXAMPLE: to have 900 samples per buffer, write N_LOC = 0x1C2.

## Inspection Mode Polarity and Shift

When the Inspection mode is enabled (bits[2:0] = 010 of register 0x8144) and bit[7] = 1 of register 0x8000, this register allows the user to configure the CHx DATA from the channels to the ROC FPGA that generates the signal on the MON/Sigma LEMO connector. Other options of the Inspection mode can be configured via register 0x8150.

NOTE: this register is supported by VME boards only.

Address        0x802A  
Mode            R/W  
Attribute       C

Bit	Description
[0]	This bit manages the polarity of the CHx DATA that is transferred from the channels to the mother board ROC FPGA. Options are: 0 = signal not inverted (default); 1 = signal inverted.
[3:1]	These bits set the right shift of the CHx DATA from the 14 bits of the ADC to make it compliant with the 8 bit of the ROC FPGA. When the shift is applied, the less significant bits (LSB) are taken. Default value is 0x6, which also corresponds to the most significant bits (MSB) of the 14 bits data.
[31:4]	Reserved

## Decimation Factor

This register permits to program the decimation factor to be applied to the acquired waveforms, according to the formula  $(\text{Sampling Rate})/2^n$ , where  $n = [0, 1, \dots, 7]$ . Please, refer to the digitizer User Manual for details on this functionality. NOTE: developers not using CAEN software must consider that this register affects the post-trigger (0x8114) and the acquisition window, that is to say the record length based on the buffer organization and the custom size settings (0x800C and 0x8020).

Address        0x8044  
Mode            R/W  
Attribute       C

Bit	Description
[3:0]	n parameter
[31:4]	Reserved.

## Acquisition Control

This register manages the acquisition settings.

Address        0x8100  
 Mode            R/W  
 Attribute       C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Trigger Counting Mode Selection. Options are: 0 = only accepted triggers are counted (default); 1 = all triggers are counted.
[4]	Reserved.
[5]	Memory Full Mode Selection (default value is 0). Options are: 0 = NORMAL. The board is full whenever all buffers are full; 1 = ONE BUFFER FREE. The board is full whenever Nb-1 buffers are full, where Nb is the overall number of buffers in which the channel memory is divided.
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Busy signal as input, or to propagate it as output. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.

[9]	<p>LVDS I/O Veto Enable (VME only). Default value is 0.</p> <p>The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output.</p> <p>Options are:</p> <p>0 = disabled (default);</p> <p>1 = enabled.</p> <p>NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.</p>
[10]	Reserved.
[11]	<p>LVDS I/O RunIn Enable Mode (VME only). Default value is 0.</p> <p>The LVDS I/Os can be programmed to accept a RunIn signal as input, or to transfer it as output.</p> <p>Options are:</p> <p>0 = starts on RunIn level (default);</p> <p>1 = starts on RunIn rising edge.</p> <p>NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 must also be configured for nBusy/nVeto.</p> <p>NOTE: This register is valid from ROC FPGA fw revision 4.16 on.</p>
[12]	<p>Enable extended VetoIn option to inhibit TRGOUT generation (VME only). The veto signal on the LVDS is generated with a programmable delay (extended Veto duration is set by 0x81C4 register).</p> <p>Options are:</p> <p>0 = Extended Veto not used (default)</p> <p>1 = Extended Veto used for TRGOUT inhibit</p> <p>NOTE: this bit is reserved in case of Desktop and NIM digitizers or ROC FPGA firmware rel. &lt;= 4.16 .</p>
[31:13]	Reserved.

## Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address      0x8104  
 Mode         R  
 Attribute    C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved.



## Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address        0x8108  
Mode            W  
Attribute       C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

## Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address        0x810C  
 Mode           R/W  
 Attribute      C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from channel n (n = 0,...,3 for DT, and NIM boards; n = 0,...,7 for VME boards) that participates to the global trigger generation. Options are: 0 = Trigger request does not participate to the global trigger generation; 1 = Trigger request participates to the global trigger generation. NOTE: in case of DT and NIM boards bits[7:4] are reserved.
[19:8]	Reserved. NOTE: in case of DT and NIM boards, bits[19:4] are reserved.
[23:20]	Majority Coincidence Window. Sets the time window (10 ns steps) for the majority coincidence. Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. For a level m, the trigger fires when at least m+1 of the enabled trigger requests (bits[7:0] or [3:0]) are over-threshold inside the majority coincidence window (bits[23:20]). NOTE: The majority level must be smaller than the number of channel enabled via bits[7:0] mask (or [3:0]).
[27]	TRG-IN used as gate. When enabled the TRG-IN is in logic AND with the channel self-trigger, which acquire when TRG-IN is high. Options are: 0 = TRG-IN in logic OR with the enabled channels and SW trigger (default); 1 = TRG-IN in logic AND the enabled channels. NOTE: this bit must be used in conjunction with bit[10] of register 0x811C. NOTE: this bit is reserved for ROC FPGA firmware release less than 4.9.
[28]	Reserved.
[29]	LVDS Trigger (VME boards only). When enabled, the trigger from LVDS I/O participates to the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

## Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address        0x8110  
 Mode            R/W  
 Attribute       C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from channel n (n=0,...,3 in case of DT and NIM boards; n = 0,..., 7 in case of VME boards) that participates to the TRG-OUT (GPO) signal. Options are: 0 = Trigger request does not participate to the TRG-OUT (GPO) signal; 1 = Trigger request participates to the TRG-OUT (GPO) signal. NOTE: In case of DT and NIM boards bits [7:4] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests (bits [7:0] or [3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are between 0 and 7 for VME boards, and between 0 and 3 for DT and NIM boards. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [7:0] or [3:0]) .
[28:13]	Reserved.
[29]	LVDS Trigger Enable (VME boards only). If the LVDS I/Os are programmed as outputs, they can participate in the TRG-OUT (GPO) signal generation. They are in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

## Post Trigger

The value of this register is used to set the number of post-trigger samples, that is the number of further samples that are written by the FPGA in the channel memory, when a trigger occurs, before to freeze the buffer. The number of post trigger samples is:

$$N_{\text{post}} = \text{PostTriggerValue} \cdot 2 + \text{ConstantLatency}$$

where:

$N_{\text{post}}$  = number of post trigger samples.

PostTriggerValue = content of this register.

ConstantLatency = constant number of added samples due to the latency associated to the trigger processing logic in the ROC FPGA. This value is constant, but the exact value may change between different firmware revisions.

Address	0x8114
Mode	R/W
Attribute	C

Bit	Description
[31:0]	PostTriggerValue

## LVDS I/O Data

This register allows to readout the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs (REGISTER mode).

NOTE: this register is supported by VME boards only.

Address        0x8118  
Mode            R/W  
Attribute       C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). If the LVDS I/O new features are enabled (bit[8] of 0x811C) and REGISTER mode is set (through 0x81A0), this register allows to read/write from the corresponding nth LVDS I/O according to its configuration. A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input.
[31:16]	Reserved.

## Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address        0x811C  
 Mode          R/W  
 Attribute     C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. NOTE: this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards and LVDS I/O old features only). This configuration must be enabled through bit[8] set to 0. Options are: 00 = general purpose I/O; 01 = programmed I/O; 10 = pattern mode: LVDS signals are input and their value is written into the header PATTERN field; 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.

[8]	<p>LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.</p>
[9]	<p>LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. NOTE: this bit is reserved in case of DT and NIM boards.</p>
[10]	<p>TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.</p>
[11]	<p>TRG-IN to Mezzanines (channels). Options are: 0 = the TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. NOTE: if this bit is set to 1, then bit[10] is ignored.</p>
[13:12]	Reserved.
[14]	<p>Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.</p>
[15]	<p>TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1 = TRG-OUT (GPO) is a test logic level set via bit[14].</p>
[17:16]	<p>TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.</p>
[19:18]	<p>Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].</p>

[20]	<p>According to bits[19:18], this bit selects the probe to be propagated on TRG- OUT .</p> <p>If bits[19:18] = 00, then bit[20] options are:</p> <p>0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT-&gt;TR-IN or TRG-OUT-&gt;S-IN (GPI) daisy chain.</p> <p>1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards).</p> <p>If bits[19:18] = 11, then bit[20] options are:</p> <p>0 = Board BUSY;</p> <p>1 = PLL Lock Loss.</p> <p>NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower.</p> <p>NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.</p>
[22:21]	<p>Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (TRG OPTIONS field in case of DT and NIM boards).</p> <p>Option are:</p> <p>00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default);</p> <p>NOTE: 00 is meaningless in case of DT and NIM boards.</p> <p>01 = EVENT TRIGGER SOURCE: 16-bit PATTERN/TRG OPTIONS indicates the trigger source causing the event acquisition;</p> <p>10 = EXTENDED TRIGGER TIME TAG: enables the Trigger Time Tag information over 48 bits. The 16 most significant bits are given by the 16-bit PATTERN/TRG OPTIONS field, while the remaining 32 ones are given by the TRIGGER TIME TAG information in the header of the event format (roll-over bit is not managed).</p> <p>11 = NOT USED: if configured, it acts like 00 setting.</p> <p>NOTE: Refer to the Event Structure section of the digitizer User Manual for a complete information.</p>
[31:23]	Reserved.



## Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.

WARNING: this register must not be modified while the acquisition is running.

Address        0x8120  
Mode            R/W  
Attribute       C

Bit	Description
[7:0]	Channel Enable Mask. Default value is 0xFF. Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled. NOTE: bits[15:8] are reserved in case of DT and NIM boards.
[31:8]	Reserved.

## ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.

EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

## Event Stored

This register contains the number of events currently stored in the Output Buffer.

NOTE: the value of this register cannot exceed the maximum number of available buffers according to the register address 0x800C.

Address        0x812C  
Mode            R  
Attribute       C

Bit	Description
[31:0]	Number of the current events stored in the Output Buffer.

## Voltage Level Mode Configuration

When the Voltage Level Mode is enabled (bit[2:0] = 100 of register 0x8144), this register sets the DAC value to be provided on the front panel MON/Sigma output LEMO connector: 1 LSB = 0.244 mV, terminated on 50 Ohm.

NOTE: this register is supported by VME boards only.

Address        0x8138  
 Mode           R/W  
 Attribute      C

Bit	Description
[11:0]	DAC Voltage Setting (VME boards only). The corresponding output value is multiplied by 0.244 mV.
[31:12]	Reserved

## Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.

A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.

EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

NOTE: this register is supported by VME boards only.

NOTE: the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

## Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address        0x8140  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Digitizer Family Code: 0x0: 724 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 1: each channel is equipped with 512 kS acquisition memory; 8: each channel is equipped with 4 MS acquisition memory.
[23:16]	Equipped Channels Number. Options are: 0x2 for DT and NIM 2-ch boards; 0x4 for DT and NIM 4-ch boards; 0x8 for VME boards.
[31:24]	Reserved.

## Analog Monitor Mode

This register selects which output mode is provided on the MON/Sigma front panel LEMO connector.

NOTE: this register is supported by VME boards only.

Address        0x8144  
Mode            R/W  
Attribute       C

Bit	Description
[2:0]	Analog Monitor Mode (VME boards only). Options are: 000 = Trigger Majority mode; 001 = Test mode; 010 = Inspection mode; 011 = Buffer Occupancy mode; 100 = Voltage Level mode; Others = reserved. Please, refer to the digitizer User Manual for a detailed description.
[31:3]	Reserved.

## Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address        0x814C  
Mode            R  
Attribute       C

Bit	Description
[31:0]	Event Size (32-bit words).



## Inspection Mode Configuration

When the Inspection mode is enabled (bits[2:0] = 010 of register 0x8144) and bit[7] = 1 of register 0x8000, this register allows the user to configure the signal on the MON/Sigma LEMO connector. Other options can be configured via register 0x802A.

NOTE: this register is supported by VME boards only.

Address        0x8150  
Mode            R/W  
Attribute       C

Bit	Description
[7:0]	Bit n corresponds to channel n (n = 0,...,3 for DT, and NIM boards; n = 0,...,7 for VME boards) that participates to the Inspection mode. Options are: 0 = channel does not participate to the Inspection mode; 1 = channel participates to the Inspection mode. NOTE: in case of DT and NIM boards bits[7:4] are reserved.
[18:8]	Offset Value. The offset is added to the sum of the enabled channel data.
[19]	Offset Sign. Options are: 0 = positive; 1 = negative.
[21:20]	Magnify Factor. The sum of the channel data can be multiplied by a gain factor. Options are: 00 = 1x; 01 = 2x; 10 = 4x; 11 = 8x.
[30:22]	Reserved.
[31]	Inspection inverter. Options are: 0 = 1x; 1 = -1x.

## Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.

NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).

Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.

NOTE: this register is supported by Desktop (DT) boards only.

Address            0x8168  
 Mode              R/W  
 Attribute         C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

## Memory Buffer Almost Full Level

This register allows to set the level for the Almost Full generation. The written value (ALMOST FULL LEVEL) represents the number of buffers that must be full of data before to assert the BUSY signal. This register takes part in the BUSY propagation among multiple boards.

NOTE: if this register is set to 0, the ALMOST FULL is a FULL.

For the Almost Full description, please refer to the Acquisition Synchronization section of the digitizer User Manual.

Address        0x816C  
Mode            R/W  
Attribute       C

Bit	Description
[10:0]	ALMOST FULL LEVEL.
[31:11]	Reserved.

## Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG- IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address        0x8170  
Mode            R/W  
Attribute       C

Bit	Description
[7:0]	Delay value in steps of 20 ns.
[31:8]	Reserved.

## Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.

NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address        0x8178  
Mode            R  
Attribute       C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

## Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).

Options are:

- 1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
- 2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;
- 3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun );
- 4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.

Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.

NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.

NOTE: this register is supported by VME boards only.

Address        0x81A0  
Mode            R/W  
Attribute      C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration.
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	<p>This bit permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG- OUT connector or a copy of the acquisition common trigger.</p> <p>Options are:</p> <p>0 = nTrigger output is a copy of TRG-OUT signal</p> <p>1 = nTrigger output is a copy of the acquisition common trigger.</p> <p>NOTE: this bit is reserved for ROC FPGA firmware revisions less than 4.9.</p>
[31:17]	Reserved.

## Buffer Occupancy Gain

If the Buffer Occupancy Mode is selected (bit[2:0] = 011 of 0x8144), the LEMO MON/Sigma output connector provides a voltage level whose amplitude increases in fixed steps exactly with the number of events in the event buffer. Each step of the output voltage level is 0.976 mV. A gain can be applied to the step by this register. Allowed values are in the range [0:A]. The default value, 0, means no gain applied while writing 0xn means that the fixed step is -2 mV.

NOTE: this register is supported from ROC FPGA firmware revision 4.9 on.

NOTE: this register is supported by VME boards only.

Address        0x81B4  
Mode            R/W  
Attribute       C

Bit	Description
[3:0]	Buffer Occupancy Gain.
[31:4]	Reserved.

## Extended Veto Delay

This register is meaningful only for VME digitizers and configures the duration of the Extended VetoIn signal for trigger inhibit when bit[12]=1 of 0x8100 register.

NOTE: This register is valid from ROC FPGA fw revision 4.16 on.

Address        0x81C4  
Mode            R/W  
Attribute       C

Bit	Description
[31:16]	Reserved.
[15:0]	Extended VetoIn duration value in units of Trigger Clock (10 ns)



## Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address        0xEF00  
 Mode            R/W  
 Attribute       C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,...,7 = sets the VME interrupt level. NOTE: these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). NOTE: this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C). NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). NOTE: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFF0 interval. NOTE: in Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or bits[31:28] of register 0xEF10. NOTE: this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

## Readout Status

This register contains information related to the readout.

Address        0xEF04  
 Mode            R  
 Attribute       C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	VME FIFO Flag. Options are: 0 = VME FIFO is not empty; 1 = VME FIFO is empty.
[31:4]	Reserved.

## Board ID

The meaning of this register depends on which VME crate it is inserted in.

In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

## MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.

NOTE: this register is supported by VME boards only.

Address        0xEF0C  
 Mode           R/W  
 Attribute      C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

## Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.

NOTE: this register is supported by VME boards only.

Address        0xEF10  
Mode            R/W  
Attribute       C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, they set the VME Base Address of the module.
[31:16]	Reserved.

## Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

NOTE: this register is supported by VME boards only.

Address        0xEF14  
Mode            R/W  
Attribute       C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

## Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address        0xEF18  
Mode            R/W  
Attribute       C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

## Max Number of Events per BLT

This register sets the maximum number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles, or block readout through USB or Optical Link).

Address        0xEF1C  
Mode            R/W  
Attribute       C

Bit	Description
[9:0]	MAX NUM EVENT PER BLT.
[31:10]	Reserved.



## Scratch

This register can be used to write/read words for test purposes.

Address        0xEF20  
Mode            R/W  
Attribute       C

Bit	Description
[31:0]	SCRATCH.

## Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address        0xEF24  
Mode            W  
Attribute       C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

## Software Clear

All the digitizer internal memories are cleared:

- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:

- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

Address            0xEF28  
Mode                W  
Attribute           C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

## Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address        0xEF34  
Mode            W  
Attribute       C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

## Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address        0xF000  
Mode           R  
Attribute      C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

## Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address        0xF004  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

## Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address        0xF008  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

## Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address        0xF00C  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.



## Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address        0xF010  
Mode           R  
Attribute      C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

## Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address        0xF014  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

## Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address        0xF018  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

## Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address        0xF01C  
Mode            R  
Attribute       C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

## Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address        0xF020  
Mode            R  
Attribute       C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

## Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address        0xF024  
Mode            R  
Attribute       C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

## Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address        0xF028  
Mode            R  
Attribute       C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

## Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address        0xF02C  
Mode           R  
Attribute      C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.



## Configuration ROM Board Version

This register contains the board version information.

Address        0xF030  
Mode           R  
Attribute      C

Bit	Description
[7:0]	Board Version Code. Options for 724 VME form factor are: V1724, VX1724: 0x11 V1724B, VX1724B: 0x40 V1724C, VX1724C: 0x12 V1724D, VX1724D: 0x41 V1724E, VX1724E: 0x42 V1724F, VX1724F: 0x43 V1724G: 0x44. Options for 724 Desktop/NIM form factor are: DT5724/N6724: 0x11 DT5724A/N6724A: 0x13 DT5724D: 0x41 DT5724E: 0x42 DT5724B/N6724B: 0x45 DT5724C/N6724C: 0x46 DT5724F/N6724F: 0x47 DT5724G/N6724G: 0x48.
[31:8]	Reserved.

## Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address        0xF034  
 Mode            R  
 Attribute       C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

## Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address        0xF038  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

## Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address        0xF03C  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

## Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address        0xF040  
Mode            R  
Attribute       C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

## Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address        0xF044  
Mode            R  
Attribute       C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

## Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address        0xF048  
Mode            R  
Attribute       C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

## Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address        0xF04C  
 Mode           R  
 Attribute      C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.



## Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Address        0xF050  
Mode            R  
Attribute       C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

## Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address        0xF080  
 Mode           R  
 Attribute      C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

## Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address        0xF084  
Mode            R  
Attribute       C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

## Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address        0xF088  
Mode            R  
Attribute       C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).



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