An Introduction to the Euroball Electronics

Aim:

This document is intended as an introduction to the Euroball electronics for users and for those who require an overview of the system. References are provided to more detailed sources of information.

Introduction:

The Euroball electronics system is a modular, open system in which there are specific cards designed for different detector types. These include Cluster detectors, Clover detectors and conventional single crystal tapered Ge detectors. The cards are built in the D-sized VXI standard [ref 1] which permits the implementation of both analogue and digital electronics in the same chassis. VXI is VMEbus with extensions to make it suitable for instrumentation by providing analogue and ECL power supplies, triggering features and larger board sizes. The selection of VXI was made on 2 grounds: firstly it is the best bus system available for building large spectroscopy systems, and secondly it recycles Eurogam's considerable investment in VXI cards and systems [ref 2]. Eurogam's use of VXI has proved that it is a suitable environment for high resolution (13 bit) gamma-ray spectroscopy electronics [ref 3]. Standards have been agreed within the European nuclear structure physics community for the use of the "user defined" VXI features [ref 4,5] and all Euroball VXI electronics adheres to these.

The VXI cards:

Up to 13 VXI cards can be located in a single VXI crate. Two of these cards are "infrastructure" cards: the Slot 0 controller (Resource Manager) [ref 6,7] and the crate readout card [ref 8]. The remaining 11 slots are usable for detector electronics although 1 slot in one crate must be allocated to the system's Master Trigger card. Detector electronics cards contain many plug-in modules which are usually vertically mounted, but can also be flat mounted. Using these plug-in modules compresses the equivalent of typically 4 to 8 crates of NIM into each VXI card. This level of integration means that the user no longer has access to the NIM front panels and switches for setup. Instead all important signals (typically more than are available on NIM front panels) are connected to computer controlled multiplexers within the VXI cards. The run-control software allows any two analogue and any two logic multiplexer outputs per crate to be connected to an oscilloscope simultaneously. Similarly all parameters to be controlled (thresholds, switches...) are computer controlled. The voltage controlled threshold or delay produced by any DAC output can be read directly by an ADC in the Slot 0/Resource Manager card in each VXI crate via a multiplexed voltage inspection line.

VXI cards used in Euroball are:

- Slot 0 controller/Resource Manager.
- Clover Detector card (4 Ge channels + 1 spare + a BGO shield channel) [ref 9]
- Cluster Ge card (7 Ge channels + 1 spare) [ref 10]
- Cluster BGO card (18 BGO channels + 1 spare + 1 sum energy channel) [ref 10]
- Master Trigger card

- Crate readout card (STR8080)
- Neutron detector card (to be confirmed)
- Si ball detector card (to be confirmed)
- Tapered Ge card (6 channels) [ref 11]
- BGO shield card (6 channels, for use with tapered Ge card) [ref 12]

A Cluster PPADC card (8 Ge channels) is also under development using the new concept of entirely digital pulse processing [ref 13,14]

System Architecture

The Euroball system comprises 9 VXI crates for the main escape suppressed Ge detectors plus a crate each for Neutron detector electronics and for Si detector electronics, giving a total of 11 VXI crates handling over 1000 detector output signals.
Each VXI crate reads data in parallel and writes it into a buffered crate readout card where it is stored together with a sub-event header, including a 16 bit event number and an end sub-event trailer. The event number may be extended to 32 bits by use of an optional 16 bit overflow counter. Data stored in the crate readout card are transferred to the event collector over the DT32 bus [ref 15,16] and stored in VME buffers in the event collector. The DT32 readout could be configured in several ways illustrated by the following two extremes. The first is to link all crate readout cards in a daisy chain configuration and perform hardware event building by assembling all fragments of an event on the DT32 bus before writing to a single event collector buffer memory. The second is to read each event fragment (sub-event) in parallel over eleven different DT32 buses into eleven different event collector buffer memory cards, and then re-assemble them later using software. Normal operation will use a configuration somewhere between these two extremes where 2 or 3 crates will be daisy-chained onto each of 3 or 4 DT32 buses, feeding 3 or 4 VME buffer cards.

Ancillary detectors may be connected in 3 different ways. The preferred route is by designing a VXI card for a particular type of detector. This is planned for the Neutron detectors. An alternative is to use FERA ADCs and connect them either via the Eurogam FERA-DT32 interface (LeCroy 4300 QDC only) or directly to the event collector buffer memories which can have their DT32 interface module swapped for a FERA interface module. The third method is to use NIM ADCs and the Eurogam NAM (NIM ADC Module) card. This last method only works in common dead time mode (see next section).

Fig 1 on the next page shows a typical Euroball system configuration. Only 6 VXI crates are shown for clarity, and the term “detector card” covers all types of card (Ge, BGO, Cluster, Clover, Neutron, Si). A NIM and CAMAC system is shown to illustrate how non-VXI data acquisition equipment can be connected if necessary using the second method from the paragraph above involving a FERA input stage for the event collector buffer memories. One of the modules in the FERA chain would have to contain an event number counter to insert the event number into the data stream, and the last module in the chain would need to electrically buffer the Camac crate’s FERA bus to enable it to be reliably transmitted to the VME event collector. Several DT32 bus chains are shown to illustrate the possibility of having single or multiple VXI crate configurations on a DT32 bus. Trigger and control signals are not shown so as not to complicate the diagram.

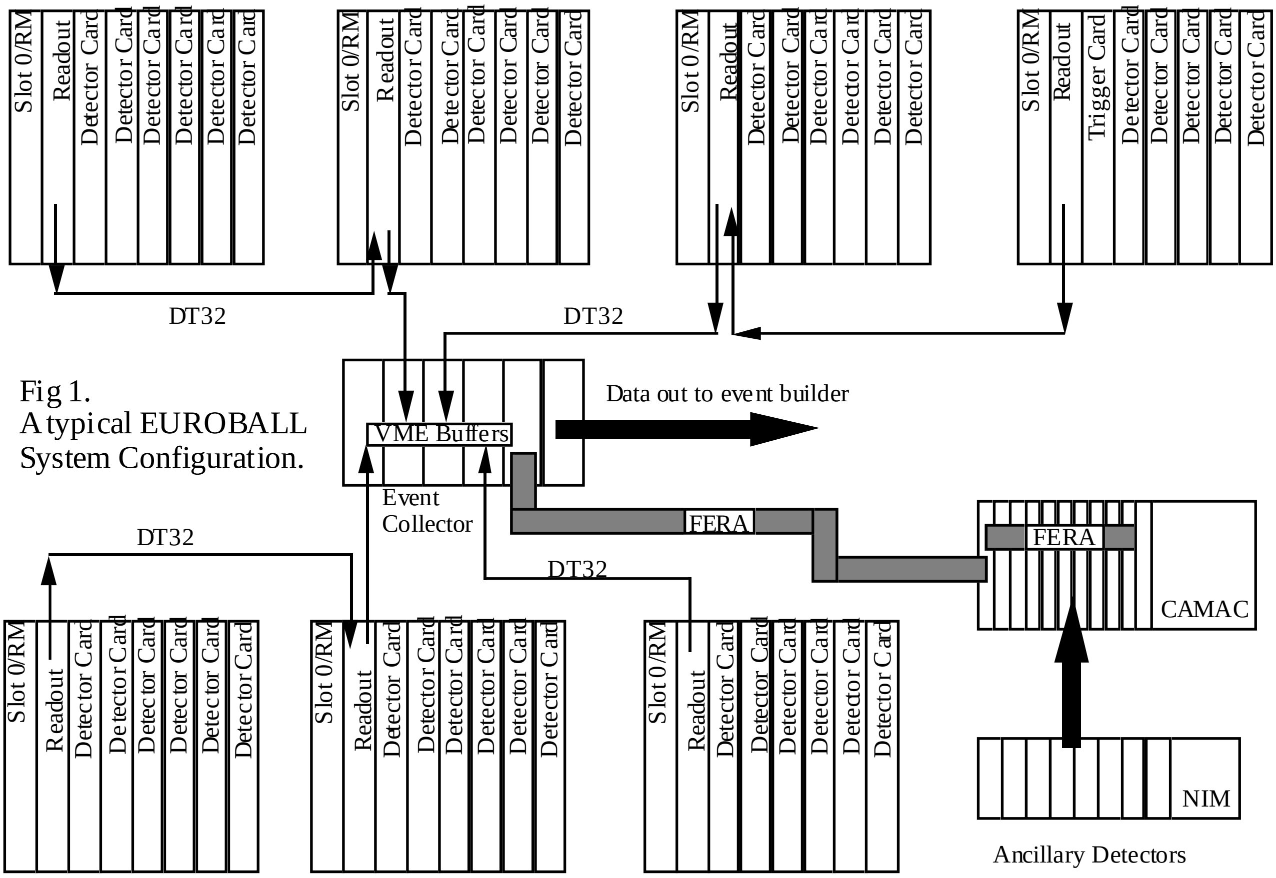


Fig 1.
A typical EUROBALL System Configuration.

System Dead time.

The Euroball system is designed to operate in parallel mode, that is more than one event being processed in parallel. The parallelism operates at the detector level for Cluster and Clover detectors i.e. if any of the detector's crystals detects a gamma-ray, the whole detector is dead until the processing of that gamma-ray is complete. For the tapered detectors from Eurogam phase 1 the detectors are grouped into three crates with 2 VXI cards (10 channels + 2 spares) in each crate and the crate is the unit of parallelism, i.e. the other 9 channels in the crate are dead while a gamma-ray detected in one channel is processed.

Both the trigger and the readout systems can operate in parallel mode. However, there is a drawback in that the efficiency will vary from event to event depending on whether or not it overlaps with another event. There are 2 cases of parallel events: overlapping and non-overlapping. In an overlapping parallel event, one or more detector will interact with gamma-rays from both the events, and will cause pileup in that detector. The effect of this pileup is to reduce the usable size of the event. In a non-overlapping event, the two events use entirely non-overlapping sets of detectors, and so do not affect each other. Even non-overlapping events may be subject to pileup from other gamma-rays not associated with the two events in question.

If constant, known efficiency is necessary for a particular experiment, then common dead time must be used as it is in Eurogam. In this case the entire array is dead (i.e. will not accept any more events) until all crates have processed their data and read them into the crate readout card. Typically this takes 15µs for 20-25 parameters in a crate. Common dead time operation is necessary if NIM ADCs are to be used with the

NAM card because of the way the NAM card controls the ADCs using their gate, select and reset signals. Common dead time operation would also be simpler to set up and control when dealing with non-VXI ancillary detectors, although parallel operation may also be used if enough preparation time is devoted to synchronising the two systems, and if variable efficiency is acceptable.

Switching between common dead time and parallel operation is achieved from software, by clicking on a button in the trigger card control window and then adjusting the inhibit signal (dead time) to select the minimum resolvable inter-event timing (see next section for more detail). No hardware changes are required.

Triggering

The Euroball trigger system was first suggested in the original Euroball proposals (ref 17) and later implemented in Eurogam (ref 18). The concept of the trigger is that each channel of electronics has some timing and logic, called a local trigger, which is programmed according to the particular experimental setup. The local trigger's timer is started by the channel's discriminator (Ge CFD, BGO LE discr...) and two programmable delays are used to test for the presence or absence of the global first and second level trigger pulses known as the fast trigger and the validation. The first level trigger occurs within 1µs of the CFD firing, and the second level trigger within 10µs of the discriminator firing. Both these global triggers must exist at the time they are sampled or tested if the channel is to complete the process of signal conversion and data readout.

Typical operation of the trigger system in common dead time and parallel mode is shown in fig 2 and 3 respectively.

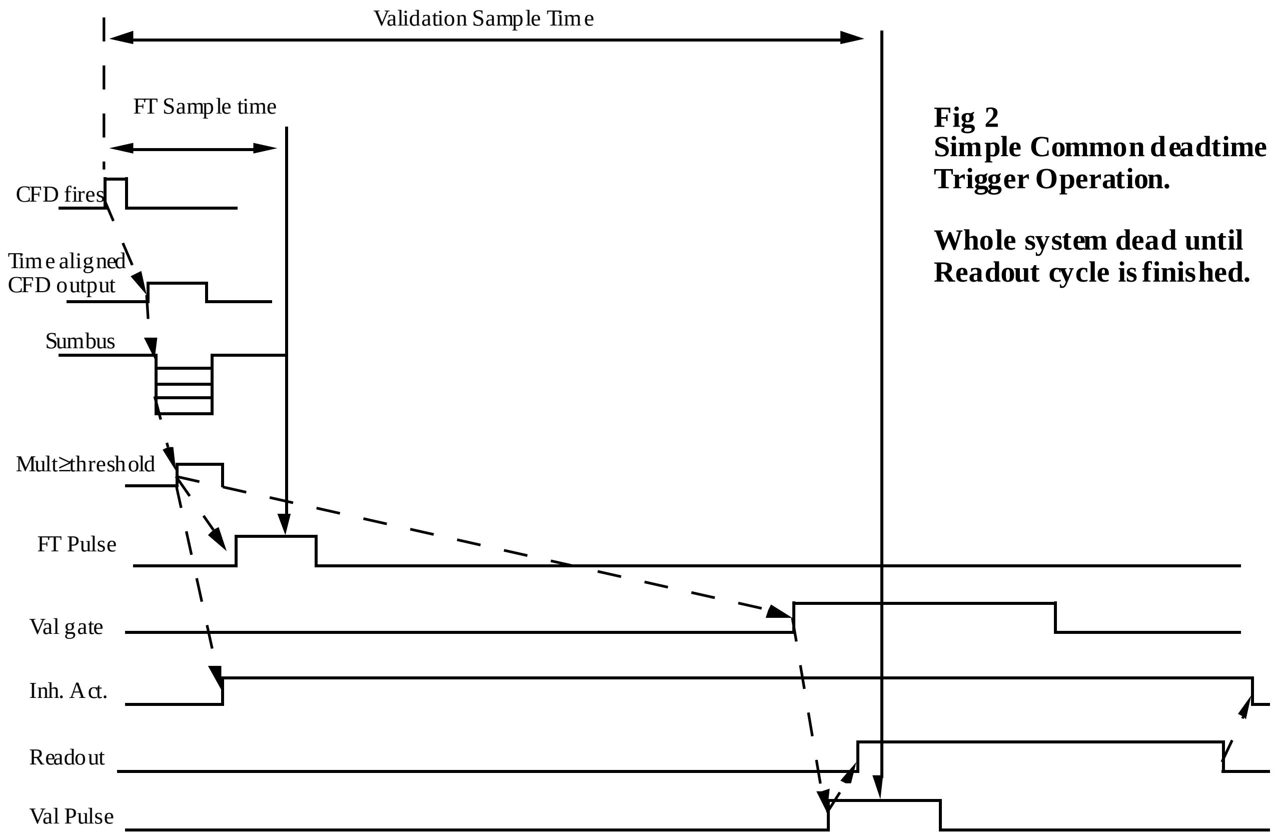
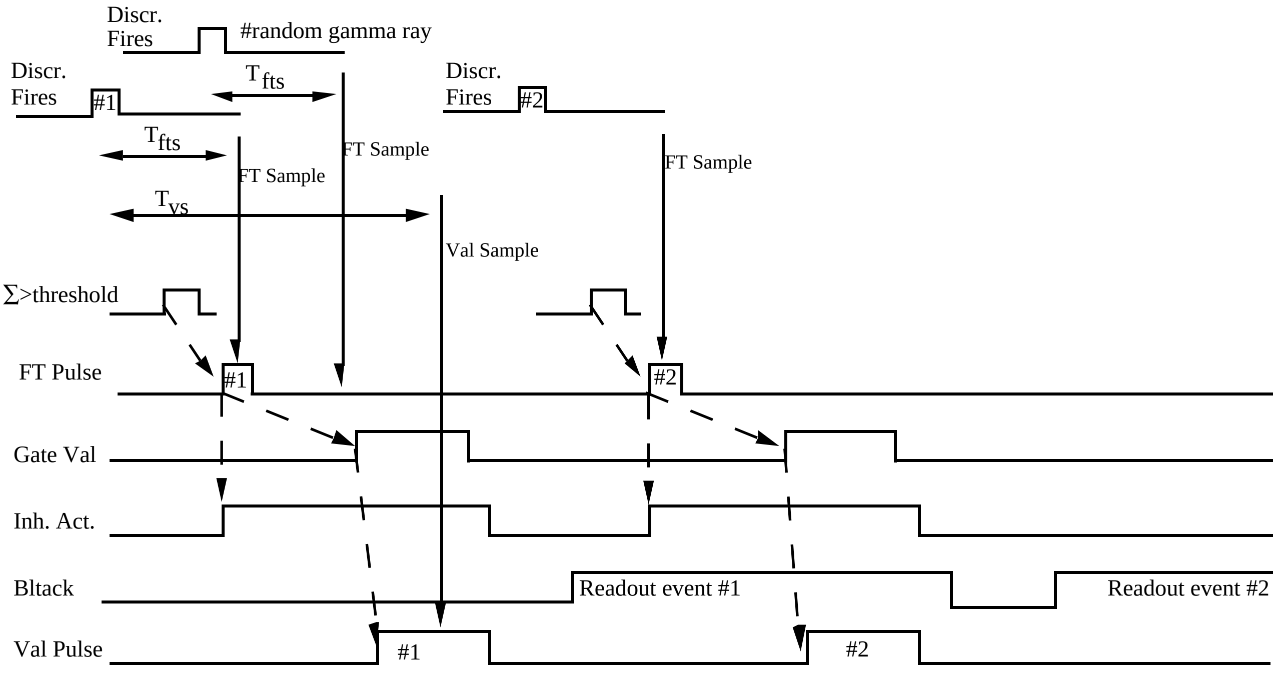


Fig 2
Simple Common deadtime Trigger Operation.

Whole system dead until Readout cycle is finished.

Euroball III Trigger
(Parallel Operation) (Fig 3)



The global fast trigger and validation trigger pulses are generated by the master trigger module as a result of a two programmable, user defined logic decisions. The signals available for the fast trigger logic are: 4 multiplicity sumbuses (Raw Ge, Clean Ge, BGO, User defined) and 6 logic inputs. For the validation logic decision a further 6 logic inputs are available. Typically only Ge multiplicity is used unless ancillary detectors are attached.

At the same time as the fast trigger, an inhibit signal is also generated by the master trigger which acts as a system dead-time indication. The width of the inhibit signal is programmable from 0-10µs and defines the minimum inter-event gap in parallel mode. In common dead time mode the inhibit signal is extended for the duration of the readout of all the VXI cards and any external ancillary detector electronics. The effect of the inhibit signal is to prevent any further triggers from being generated. There is also an input called inhibit request which may be used by users to temporarily inhibit the generation of triggers. Inhibit request should be driven by non-VXI ancillary detector electronics to extend the system dead time in common dead time mode until their data readout is complete.

Euroball Cluster Ge card.

The Euroball Cluster Germanium (Ge) card is part of the Euroball electronics system and is designed to instrument the 7 element Euroball Ge Cluster detector. The Ge card provides all the signal processing necessary to generate energy and timing data using the cluster pre-amplifier signals as inputs. The Ge card interacts with other parts of the Euroball VXI electronics for triggering, control and data readout.

Input:

8 Front panel BNC sockets to connect to Cluster Ge pre-amps.
These are 1kΩ impedance and require pre-amps with resistive feedback, 50μs time constant pulse tails (±5%), positive pulses and sensitivity of +100mV/MeV (±10%).

Signal processing for energy:

Unipolar output from 8th order quasi-trapezoidal filter with peaking time of 3μs and pulse width at 0.1% is 10μs. Output amplifier stage generates 4MeV and 20MeV ranges.

Signal processing for Timing:

TFA with 20ns integration and 180ns differentiation. TFA gain is switchable from software between x3 or x1.
CFD: min threshold 10 keV, max. threshold depends on TFA gain. For TFA gain set to x3, max threshold is 700keV adjusted in 3keV steps. For x1 TFA gain the maximum threshold is 2100keV adjusted by 8keV steps. Threshold is adjusted from software.
The CFD fraction is fixed at 0.3, and delay is fixed at 50ns.
TAC 0-2μs. (250ps resolution)

ADC

3 identical ADCs are provided per channel (per crystal) providing 3 outputs:
4MeV energy, 20MeV energy, Timing from CFD to Fast Trigger.
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5μs.
Sliding scale correction (10 bits) is used to improve the DNL to <1%. INL is <250ppm.

Triggering:

Raw and Clean Ge multiplicity outputs are provided and may be either 0/1 or 0/1/2...7 depending on whether the Cluster is to be treated as 1 composite detector or 7 discrete detectors. For Clean Ge multiplicity, a veto input is connected to the BGO shield. The Ge card accepts the 2 normal Euroball trigger pulses (Fast Trigger and Validation).

Setup:

All on-card parameters are controlled by VME cycles over the VXI bus (PZ, CFD output delay, width, CFD threshold, TFA gain, pileup threshold, readout on/off per ADC, Sliding scale on/off per ADC, trigger sampling times etc.)

Readout

Readout will take place via the Euroball GIR card [ref 19] and will support both Eurogam 32 bit wide block transfers, and Crystal Ball 64 bit SSBLT protocols.

Cluster BGO Card

The Euroball Bismuth Germanate (BGO) card is part of the Euroball electronics system and is designed to instrument the Euroball Cluster shield and back-catcher. Together, the shield and back-catcher operate as an 18 element device. The BGO card provides all the signal processing necessary to generate energy and timing data for each element. A sum channel provides the total energy, composite timing and the hit pattern. The BGO card interacts with other parts of the Euroball VXI electronics for triggering, control and data readout. A veto output is provided for the Cluster Ge card.

Input:

18 Front panel Lemo 00 sockets to connect to BGO phototube line drivers.
Negative signal with no shaping (T_r=50ns T_f=330ns). Signal level - 250mV/MeV.

Signal processing for energy:

Gated integrator with peaking time of 1µs. Output 0-20MeV.

Signal processing for Timing:

First photoelectron with validation on 2nd electron within 60ns.
TAC range 2µs, resolution 5ns.

ADC

2 identical ADCs are provided per channel (per element) providing 2 outputs:
20MeV energy, Timing from first electron to Fast Trigger.
The sum channel also provides a 20MeV energy range and a timing output from a TAC measuring from the first element firing to the Fast Trigger. A hit pattern is also generated from all elements which fired.
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5µs.
Sliding scale correction (8 bits) is used to improve the DNL to <1%. INL is <250ppm.

Triggering:

A BGO multiplicity output is provided.

Setup:

All on-card parameters are controlled by VME cycles over the VXI bus (Discriminator threshold, readout on/off per ADC, Sliding scale on/off per ADC, trigger sampling times etc.)

Readout

Readout will take place via the Euroball GIR card [ref 19] and will support both Eurogam 32 bit wide block transfers, and Crystal Ball 64 bit SSBLT protocols.

Euroball Master Trigger Card

The Master Trigger card generates the system's 2 global trigger pulses (Fast Trigger and Validation), and distributes system control signals (stop/go, inhibit, read scalers...) to each VXI crate via a ribbon cable daisy chained to each Resource Manager/slot 0 card. Another daisy chained ribbon cable provides system status to the Master Trigger card from the VXI crates via the Resource Manager/slot 0 cards.

Inputs:
4 current sumbuses. Expected level: 3.5mA/channel hit.
6 logic inputs for Fast Trigger logic
6 logic inputs for Validation logic

Thresholds:
Each of the 4 sumbuses is tested at up to 4 different thresholds, giving 16 threshold decisions in total.
The 12 logic inputs have a common logic threshold (usually fast NIM, but can be anything between ±5V).

Logic Decisions:
The Fast Trigger logic uses the 16 thresholds and the 6 logic inputs both directly and after delay/width time alignment (total 44 inputs) to make decisions about what constitutes an event. The Fast Trigger logic is contained in a Xilinx 3030 re-programmable gate array for which a library of standard set-ups exists.
The Validation logic uses the 6 Validation logic inputs both directly and after delay/width time alignment (total 12 inputs) to make decisions about whether to continue the current event to readout. In addition a 4 bit trigger type code is passed from the FT logic to the Validation logic to distinguish different trigger conditions which can be checked in parallel. The Validation logic is contained in a Xilinx 3030 re-programmable gate array for which a library of standard set-ups exists.

Outputs:
16 bit event number, trigger type word, sumbus level (x4), TAC output, measuring from one of the sumbuses crossing its threshold to front panel stop input.

Euroball Resource Manager/Slot 0 controller

This card contains a VME CPU (typically MVME147) which connects to a network (usually ethernet) to give the control software access to each VXI crate. This CPU runs the VXI crate configuration software when the VXI crate is initialised, and has access via the RM/Slot 0 controller to all necessary VXI signals such as MODID. The CPU is also the VME arbiter and system controller.

The Resource Manager card buffers two ribbon cables running to (14 way) and from (40 way) the Master Trigger carrying the system's control, status and inhibit signals to and from the VXI backplane. It also provides access to the STAR X lines for the Fast Trigger pulse, and buffers the current sumbuses on the Eurogam cards which do not use the front panel sumbus system of the newer Cluster Ge and BGO cards. Finally, the inspection lines for each VXI crate are buffered out of the front of the Resource Manager card (2 x analogue, 2 x logic, 1x voltage inspection line).

Clover VXI Card

The Clover card fully instruments a EUROGAM II Clover Ge detector and its associated BGO suppression shield. The inputs come from the Ge and BGO pre-amps and, after analogue signal processing, the output from the card is a series of energy and timing data words plus a hit pattern. A spare Ge channel is provided.

Ge Inputs:

5 front panel BNC sockets to connect to Clover Ge pre-amps. These are 1kΩ input impedance and require pre-amps with resistive feedback, 50μs time constant (+/- 5%), negative pulses and sensitivity of -200mV/MeV (±10%) from 50Ω output impedance.

Ge Signal Shaping:

Unipolar output from 6th order quasi-triangular filter with peaking time of 4.4μs and FWHM 5 μs. Pulse width at 0.1% is 11μs. An output amplifier stage generates 4MeV and 20MeV ranges. Bipolar (differentiated) outputs available for crossover timing.

Ge Timing:

TFA with 50ns integration, 180ns differentiation. Gain x3 or x10, set from software.
CFD: min threshold 20keV, pulse pair resolution better than 1μs. CFD delay 27ns.
TAC 0-2μs, FWHM 0.6ns, INL <5%

Ge ADCs

4 identical ADCs are provided per channel providing 4 outputs:
4 MeV energy, 20MeV energy, peaking time TAC and CFD to Fast Trigger TAC
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5μs.
Sliding scale correction (8 bits) is used to improve the DNL to <1%. INL is <250ppm.

BGO Input:

One 20 way IDC socket providing 8 differential inputs of 50Ω impedance. One side is grounded and the other connects to a pre-amp output with 30ns rise time constant (+/- 10%) 10μs fall time constant (+/- 1.5%) and sensitivity of +1000mV/MeV *(Phototube voltage must be adjusted to give +1000mV/MeV.)*

BGO Signal Shaping:

A summing amplifier generating a bipolar output from 4th order semi-gaussian filter ($CR^2 RC^4$, RC=2μs) is used for the BGO signal shaping.
Peaking time of 5.2μs and FWHM 5.5 μs. Pulse width at 0.1% is 12 x τ = 24μs.
Output 8 MeV full scale. Amplifier resolution is 3keV fwhm.

BGO ADCs

2 identical ADCs are provided per channel providing 2 of the 3 outputs:
8 MeV energy, CFD to Fast Trigger TAC and a hit pattern of both Ge and BGO
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5μs.
Sliding scale correction (8 bits) is used to improve the DNL to <1%. INL is <250ppm.

Readout

Readout uses on-board logic for Eurogam common dead time or Eurogam parallel readout. SSBLT readout is not supported.

Eurogam phase 1 Ge VXI Card

This card was designed to fully instrument 6 EUROGAM phase I large single crystal Ge detectors. The card is also suitable for similar GASP Ge detectors. The inputs come from the Ge pre-amps and, after analogue signal processing, the output from the card is a series of energy and timing data words.

Ge Signal Processing

Input:

6 front panel BNC sockets to connect to Clover Ge pre-amps. These are 1kΩ input impedance and require pre-amps with resistive feedback, 50µs time constant (+/- 5%), negative pulses and sensitivity of -200mV/MeV (±10%) from 50Ω output impedance. Lemo 00 inputs for Veto signals (ECL logic levels) are provided for each channel.

Signal Shaping:

Unipolar output from 6th order quasi-triangular filter with peaking time of 4.4µs and FWHM 5 µs. Pulse width at 0.1% is 11µs. An output amplifier stage generates 4MeV and 20MeV ranges. Bipolar (differentiated) outputs available for crossover timing. Hinshaw ballistic deficit correction [ref 20] is implemented.

Timing:

TFA with 50ns integration and 180ns differentiation. Gain x3 or x10.
CFD: min threshold 20keV, pulse pair resolution better than 1µs. CFD delay 50ns.
TAC 0-2µs, FWHM 0.6ns, INL <5%

ADC

4 identical ADCs are provided per channel providing 4 outputs:
4 MeV energy, 20MeV energy, peaking time TAC and CFD to Fast Trigger TAC.
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5µs.
Sliding scale correction (8 bits) is used to improve the DNL to <1%. INL is <250ppm.

Readout

Readout uses on-board logic for Eurogam common dead time readout only. Eurogam parallel readout and SSBLT readout are not supported

BGO Shield Card

This card fully instruments 6 EUROGAM phase I suppression shields. The 6 inputs connect to the 10 BGO pre-amps associated with each shield. After analogue signal processing, the output from the card is a series of energy and timing data words plus a hit pattern for each shield.

Input:

Six 20 way IDC sockets, each providing 10 differential inputs of 50Ω impedance. One side is grounded and the other connects to a pre-amp output with 30ns rise time constant (+/- 10%) 10µs fall time constant (+/- 1.5%) and sensitivity of +1000mV/MeV *(Phototube voltage must be adjusted to give +1000mV/MeV)*

Signal Shaping:

Summing amplifier adds all 10 inputs from shield and shapes the result using a 4th order semi-gaussian filter. ($CR^2 RC^4$, RC=2µs) to produce a bipolar output.
Peaking time of 5.2µs and FWHM 5.5 µs. Pulse width at 0.1% is 12 x τ = 24µs.
Output 8 MeV full scale. Amplifier resolution is 3keV fwhm.

ADC

2 identical ADCs are provided per channel providing 2 of the 3 outputs:
8 MeV energy, CFD to Fast Trigger TAC and a hit pattern of both Ge and BGO
The ADCs have 13 bits resolution (8k channels), and conversion time of 4.5µs.
Sliding scale correction (8 bits) is used to improve the DNL to <1%. INL is <250ppm.

Readout

Readout uses on-board logic for Eurogam common dead time readout only. Eurogam parallel readout and SSBLT readout are not supported

References:

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For further information about the hardware aspects of the system please contact:
Ian Lazarus (Lazarus@dl.ac.uk) or
Charles Ring (Ring@frcpn11.in2p3.fr) or
Dieter Pröhl (proehl@fz-rossendorf.de)

For information about software, and what happens in and after the event collector, please contact
Gaetano Maron (Maron@lnl.infn.it) or
Vic Pucknell (Pucknell@dl.ac.uk).

Euroball Electronics and Data Acquisition Chairman: Francis Beck (Beck@frcpn11.in2pr.fr)